1 Cover Sheet
2 System Block Diagram
3 Intel LGA775 CPU - Signals
4 Intel LGA775 CPU - Power
5 Intel LGA775 CPU - GND
6 nVidia C55 - CPU / PCI-E
7 nVidia C55 - HT Link / Power
8 nVidia C55 - Memory A0
9 nVidia C55 - Memory A1
10 nVidia C55 - Gnd
11 DDR II DIMM 1 & 2
12 DDR II DIMM 3 & 4
13 DDR II Termination / EMI
14 nVidia BR04 - C55 Side
15 nVidia BR04 - PCIE x16 Slot
16 nVidia BR04 - Power / Gnd
17 nVidia MCP55 - HT / PCI / LPC
18 nVidia MCP55 - PCI-E
19 nVidia MCP55 - SATA / IDE / RGMII
20 nVidia MCP55 - Audio / USB / GPIO
21 nVidia MCP55 - PWR & GND
22 NB PCI-E x16 Pri / Sec Slot
23 SB PCI-E x16 Pri / Sec Slot
24 SB PCI-E x1 / PCI Slot
25 Gigabit PHY - RTL8211B
26 1394 Controller - JMB381
27 Azalia Codec - ALC885
28 JMicron JMB363
29 Super I/O - F71882FG
30 Fan Controller
31 MS12 ACPI Controller
32 uPI Power Regulator
33 VRD11- ISL6322 8 Phase
34 Front / Rear USB Connectors
35 ATX / Front Panel / LED
36 Manual Parts
37 Power On/Off Sequence
38 System Reset Map
39 Syatem Power Map
40 GPIO & Jumper Setting
41 Project History

MS-7510 Version : 0A Diamond Edition

CPU :

Intel Conroe Family and Kentsfield Family Processor
Intel Pentium D Processor 900 and 800 Sequence
Intel Pentium 4 Processor 600 Sequence

System Chipset :

nVidia C72XE [C55 + BR04]
nVidia MCP55P

On Board Chipset :

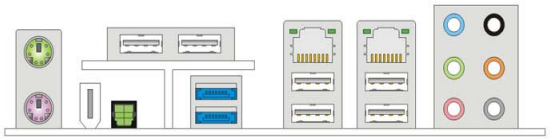
Azalia Codec - RealTek ALC885
GB PHY 1 -- RealTek RTL8211BL
GB PHY 2 -- RealTek RTL8211BL
VRM 11 - Intersil ISL6322
ACPI Controller -- MS12
IEEE 1394a Controller -- JMicron JMB381
eSATA Controller -- JMicron JMB363
Super I/O -- FinTek F71882FG
SPI Flash 8Mb

Main Memory :

2 Channel DDR II * 4 (Max 8GB)

Expansion Slot :

PCI Express x16 Slot * 3
PCI Express x8 Slot * 1
PCI Express x1 Slot * 2
PCI Slot * 1



ERP No.	Config Item	PlatForm or Option	Option Select
7510-A10	Cfg-STD	C55 + BR04 + MCP55P + ALC885 + RTL8211BP + JMB381 + JMB363 + F71882FG	STD

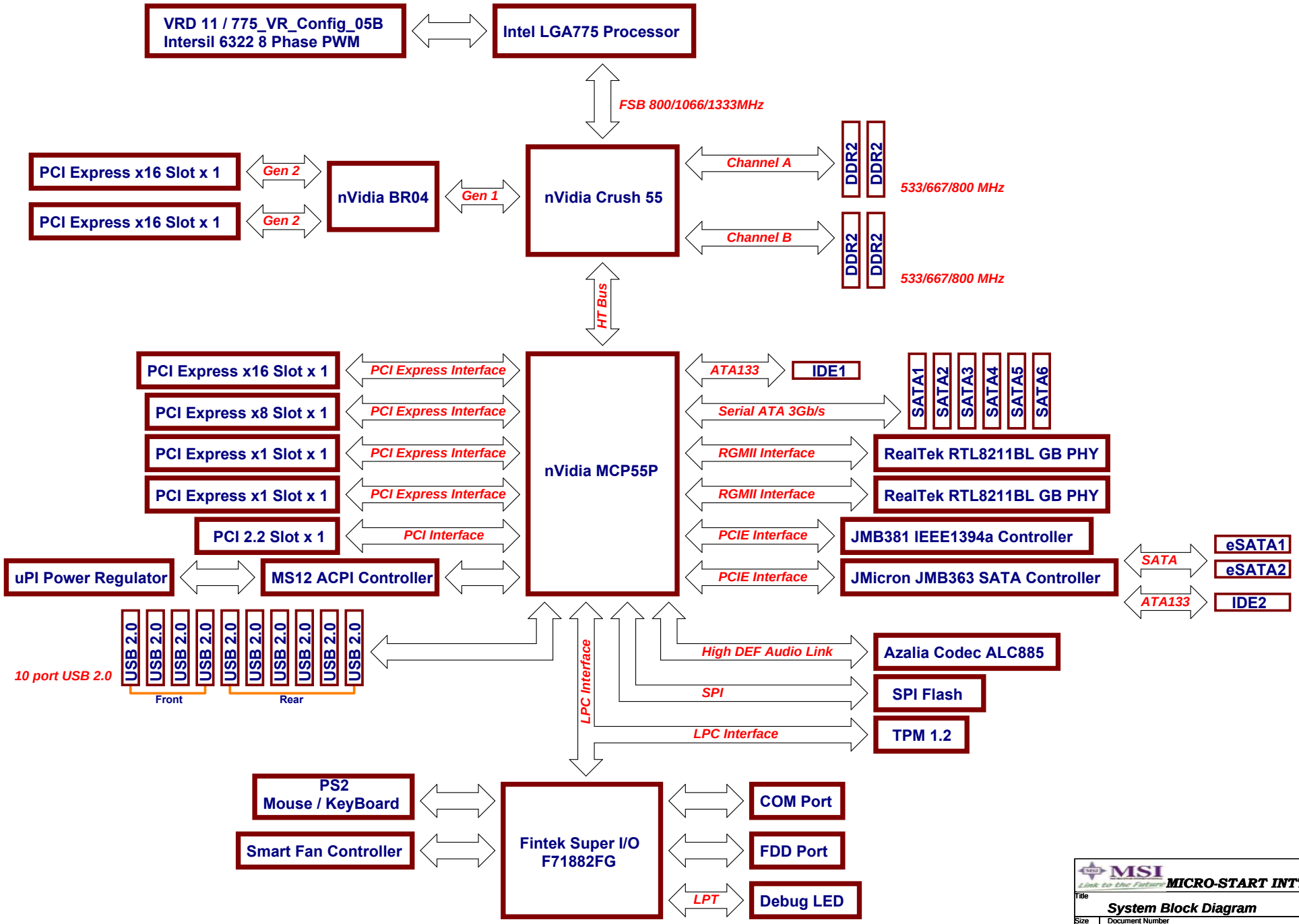
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Cover Sheet

Size | Document Number: MS-7510 | Rev: 0A

Date: Friday, September 07, 2007 Sheet 1 of 41

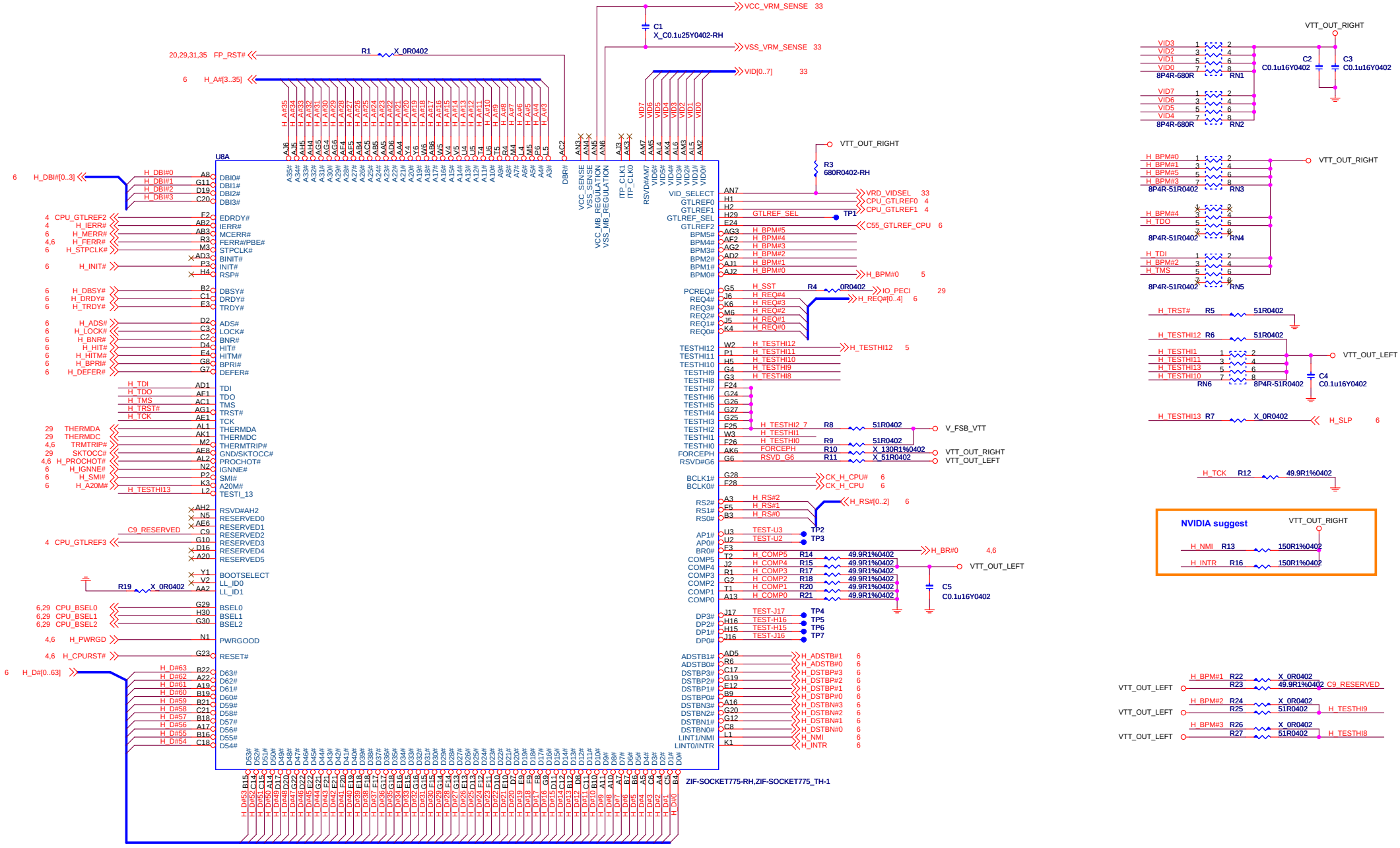
System Block Diagram



MICRO-START INT'L CO.,LTD.

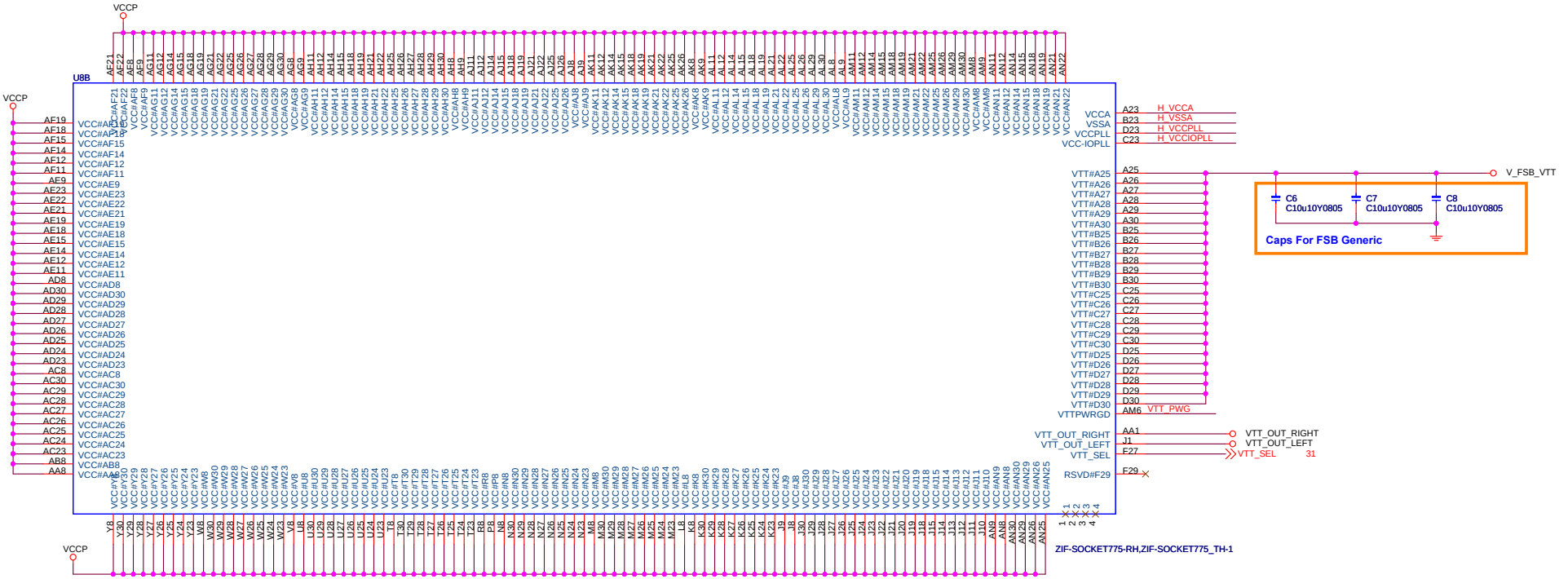
Title: System Block Diagram		
Size	Document Number: MS-7510	Rev: 0A
Date: Friday, September 07, 2007	Sheet 2 of 41	

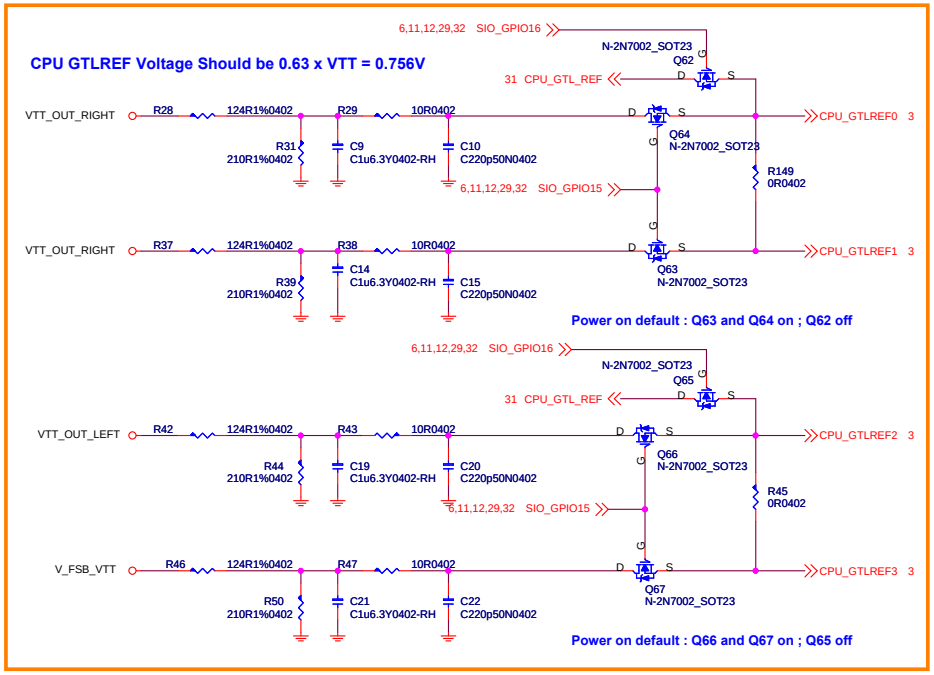
CPU LGA775 - Signals

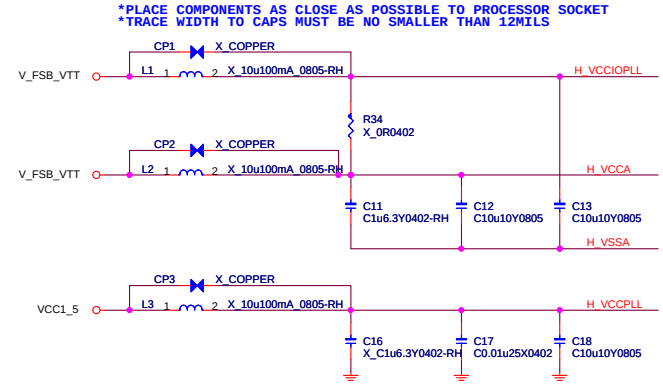


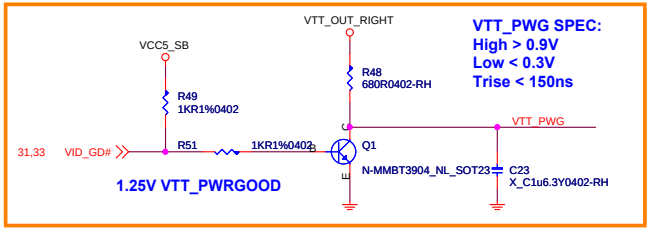
MICRO-START INT'L CO.,LTD.			
Title: CPU LGA775 - Signals			
Size	Document Number: MS-7510		Rev: 0A
Date: Friday, September 07, 2007	Sheet 3 of 41		

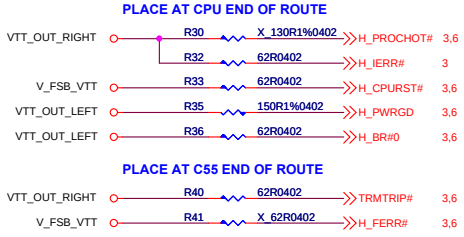
CPU LGA775 - Power







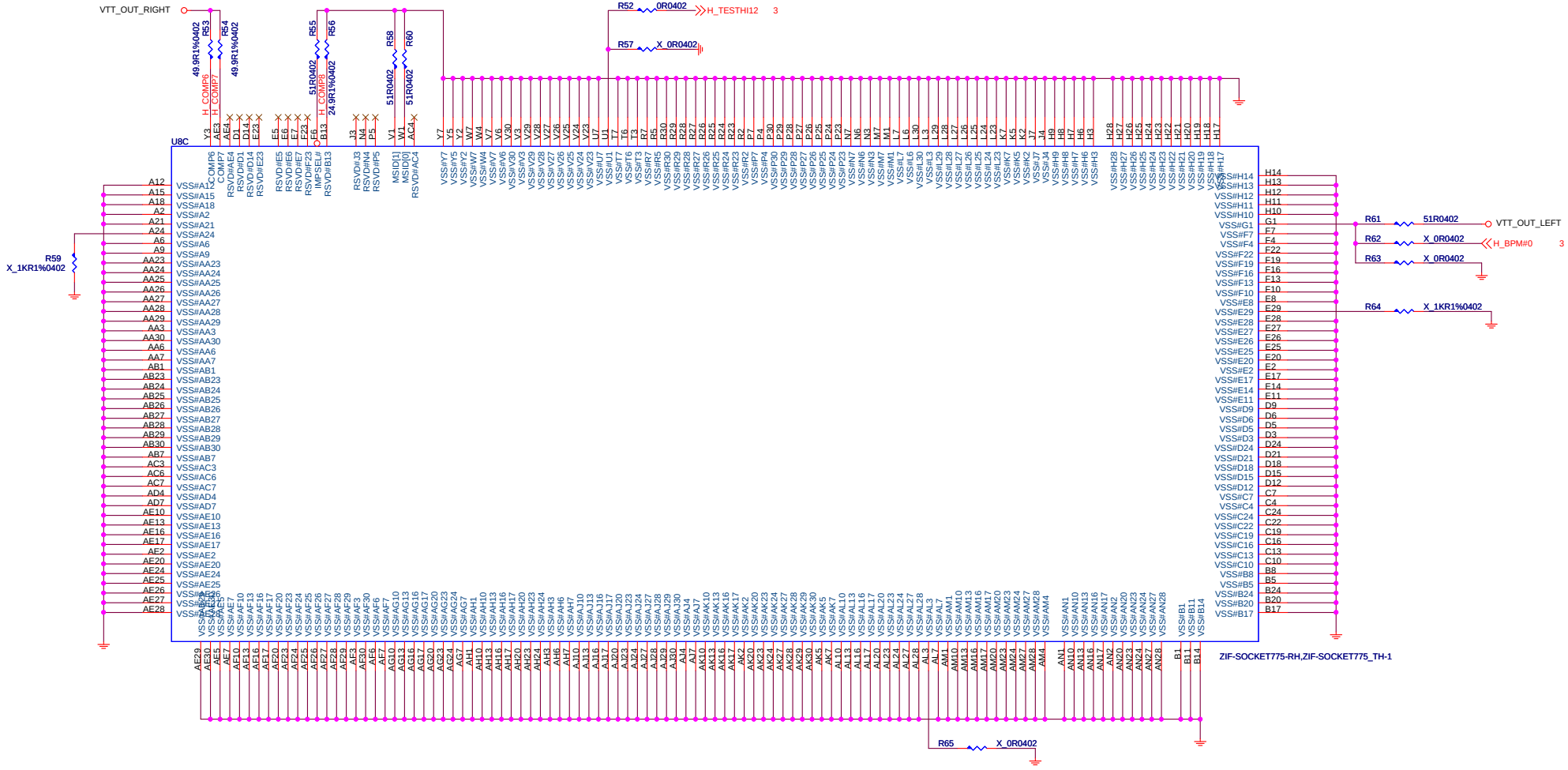




MICRO-START INT'L CO.,LTD.

Title	CPU LGA775 - Power	
Size	Document Number MS-7510	Rev 0A
Date: Monday, September 10, 2007	Sheet 4 of 41	

CPU LGA775 - Gnd

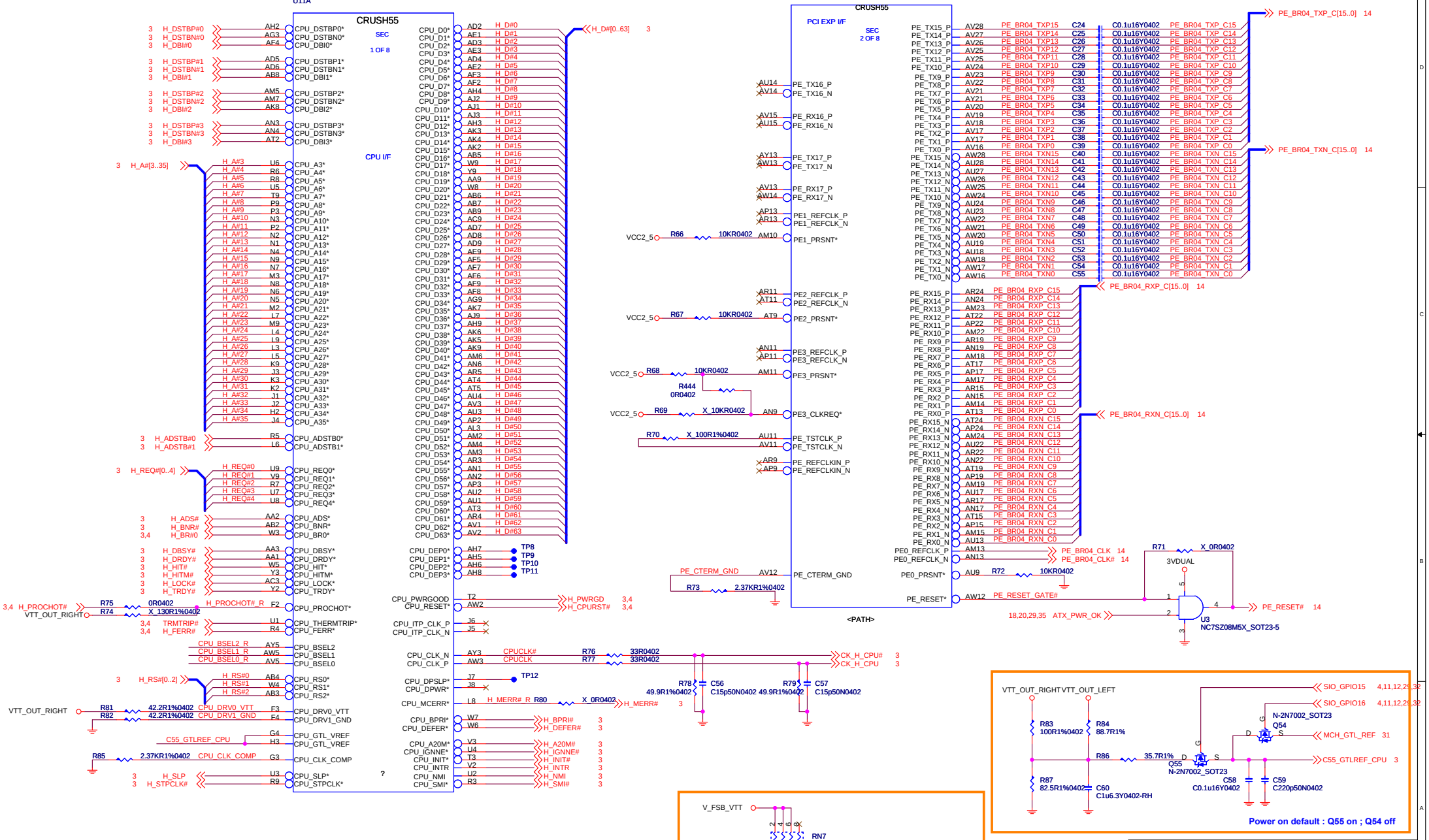


MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title	CPU LGA775 - Gnd	
Size	Document Number: MS-7510	Rev: 0A
Date: Friday, September 07, 2007	Sheet 5 of 41	

C55 - CPU / PCI-E

U11A — CRUSH55 — SEC 1 OF 8 — CPU I/F

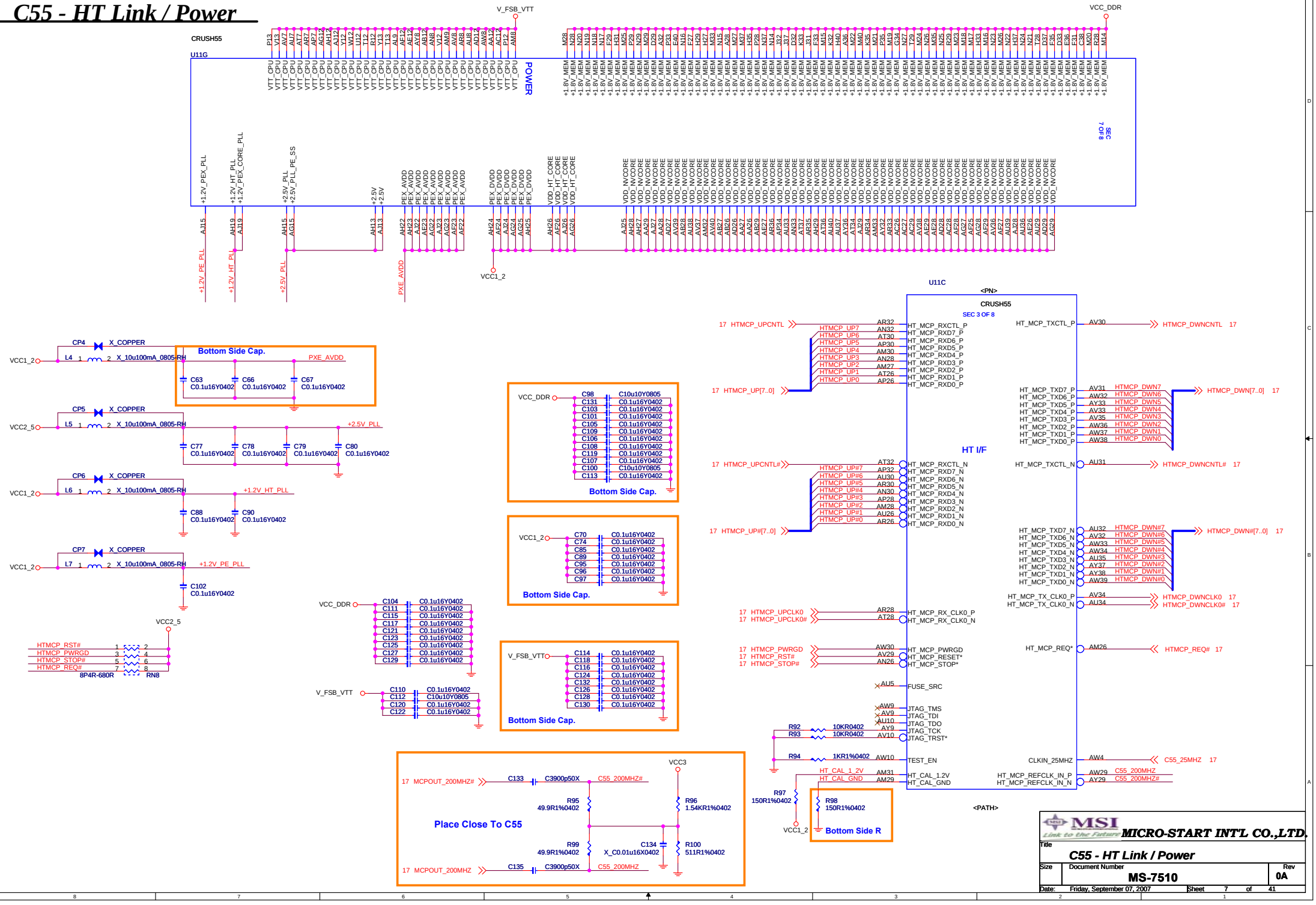
U11B — CRUSH55 — PCI EXP I/F — SEC 2 OF 8



Title	C55 - CPU / PCI-E		
Size	Document Number		Rev
	MS-7510		0A
Date: Friday, September 07, 2007		Sheet 6 of 41	

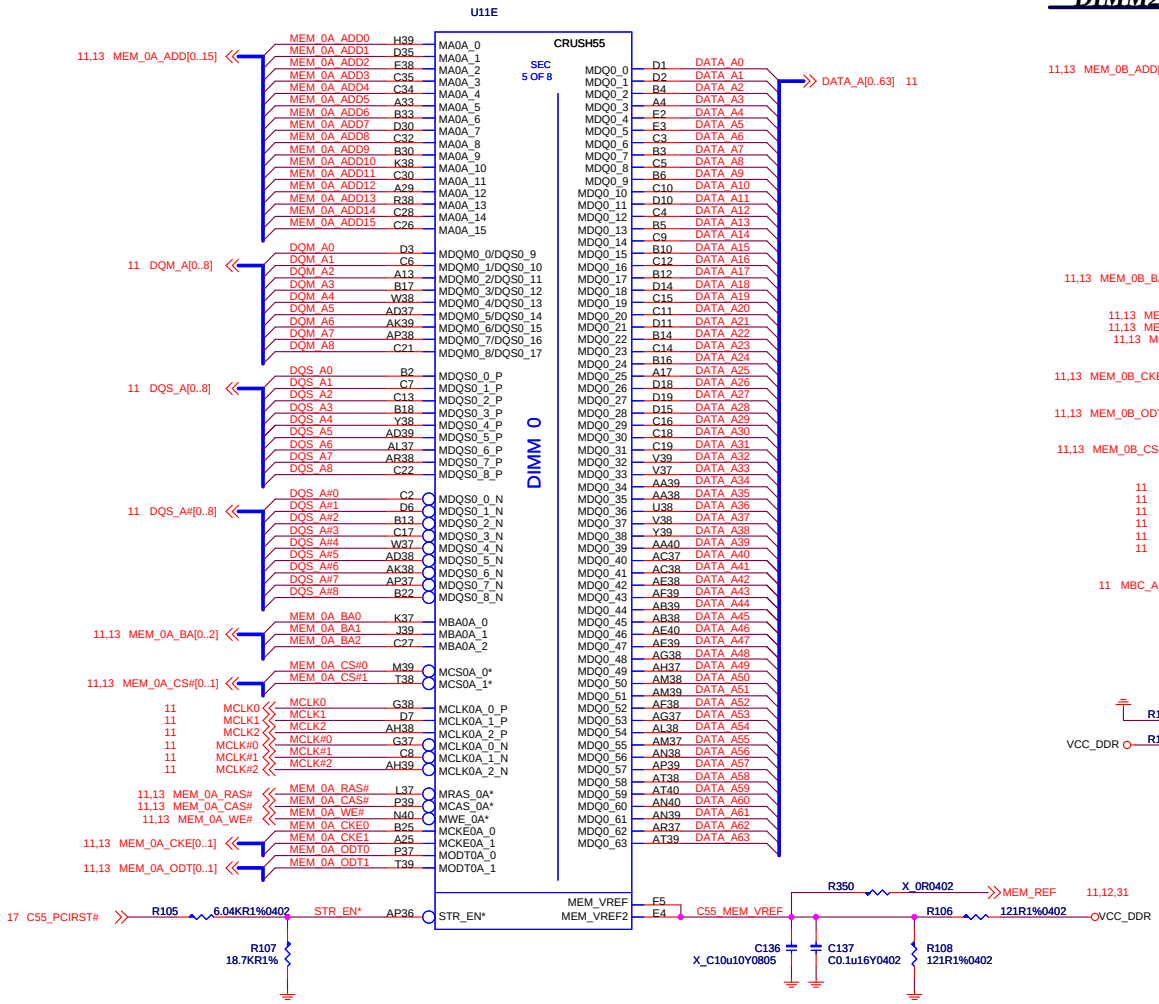
MICRO-START INT'L CO.,LTD.

C55 - HT Link / Power

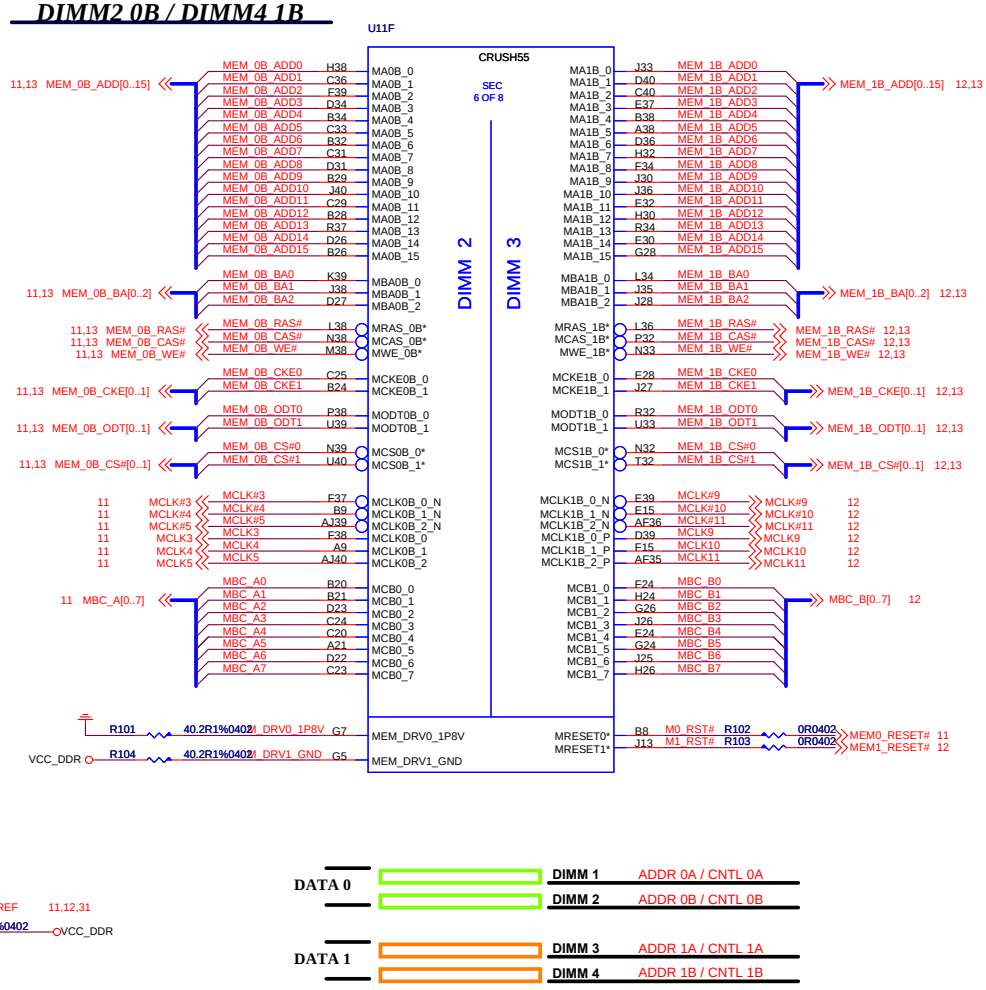


C55 - Memory A0

DIMM1 0A



DIMM2 0B / DIMM4 1B



DATA 0
- DIMM 1 ADDR 0A / CNTL 0A
- DIMM 2 ADDR 0B / CNTL 0B

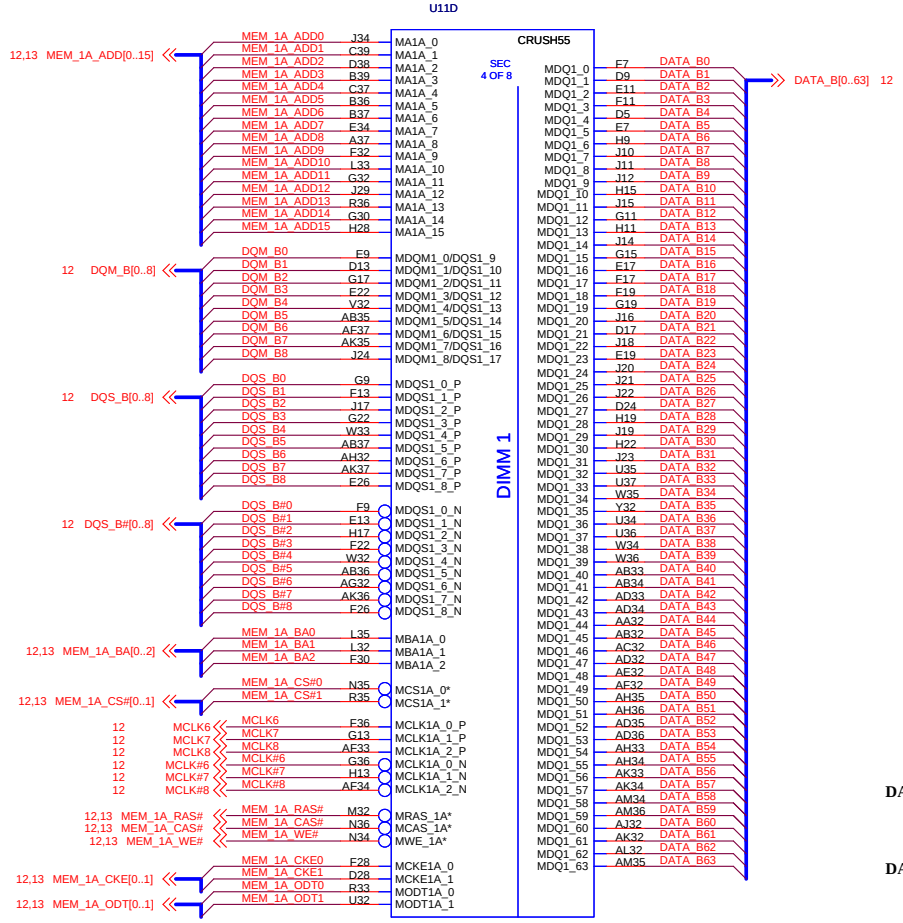
DATA 1
- DIMM 3 ADDR 1A / CNTL 1A
- DIMM 4 ADDR 1B / CNTL 1B

MICRO-START INT'L CO.,LTD.

Title	C55 - Memory A0	
Size	Document Number MS-7510	Rev 0A
Date: Friday, September 07, 2007	Sheet 8 of 41	

C55 - Memory A1

DIMM3 1A



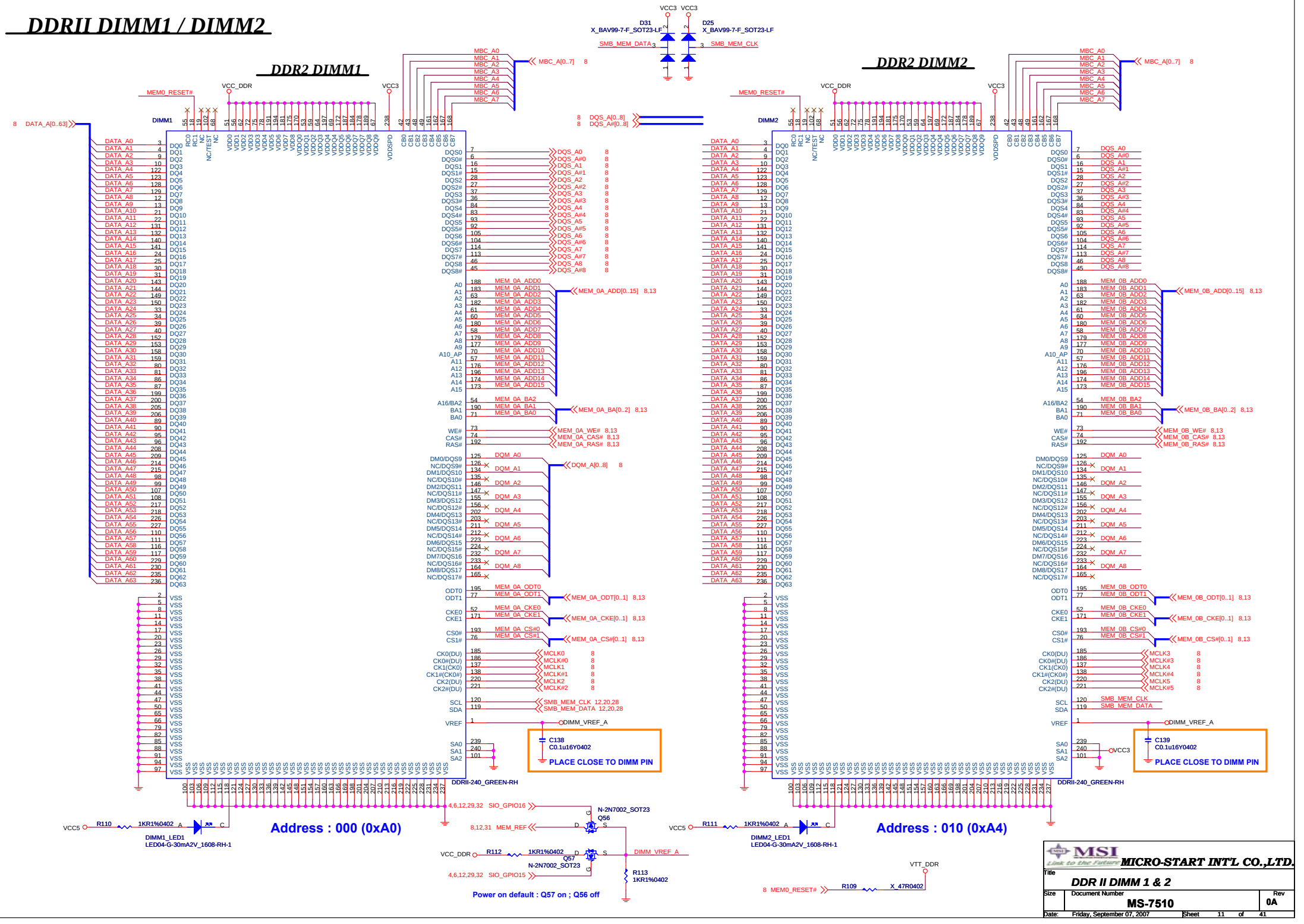
MICRO-START INT'L CO.,LTD.

Title	C55 - Memory A1	
Size	Document Number MS-7510	Rev 0A
Date: Friday, September 07, 2007	Sheet 9 of 41	

C55 - Gnd

MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	C55 - Gnd		
Size	Document Number	MS-7510	Rev 0A
Date: Friday, September 07, 2007	Sheet 10 of 41		

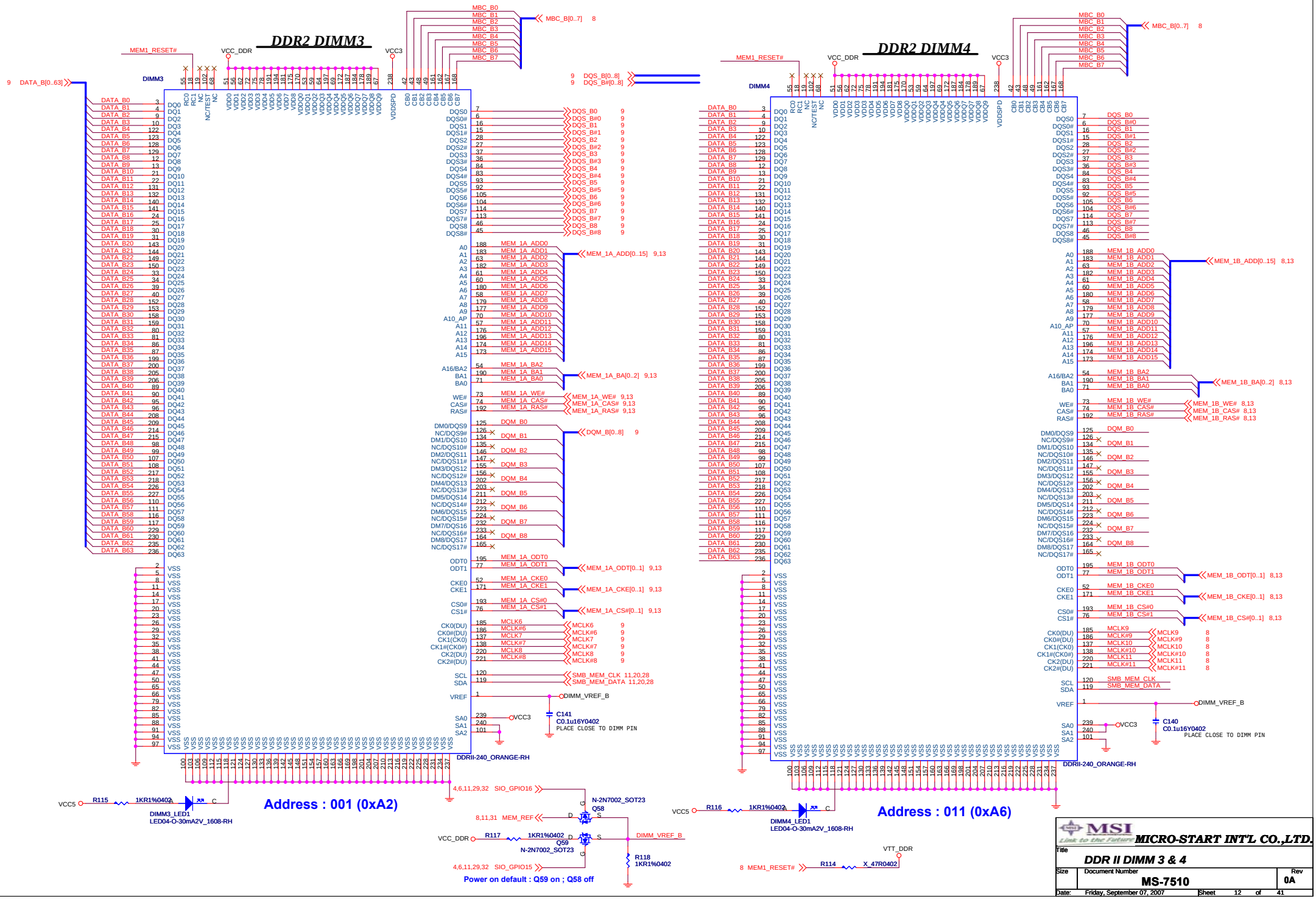
DDRII DIMM1 / DIMM2



MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title	DDR II DIMM 1 & 2	
Size	Document Number MS-7510	Rev 0A
Date: Friday, September 07, 2007	Sheet 11 of 41	

DDRII DIMM3 / DIMM4

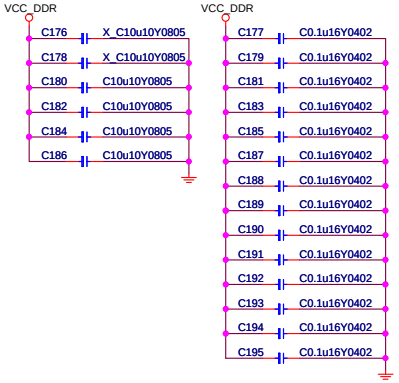


MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

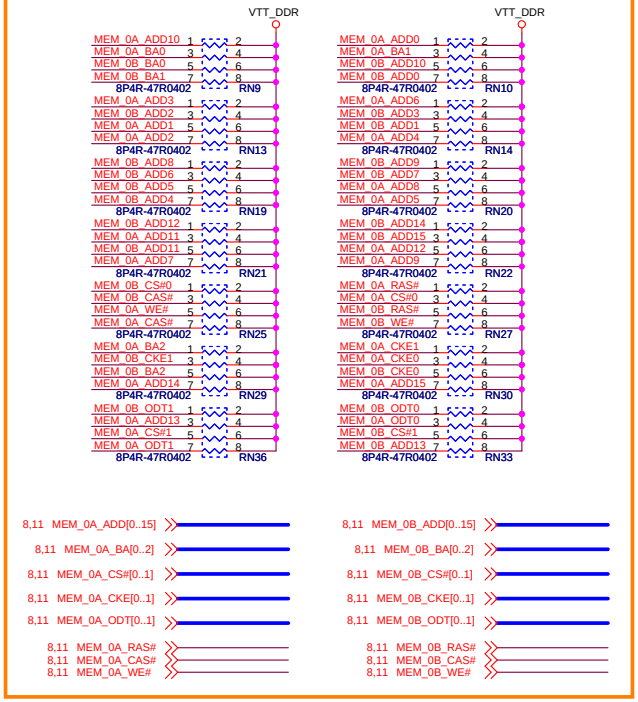
Title	DDR II DIMM 3 & 4	
Size	Document Number MS-7510	Rev 0A
Date: Friday, September 07, 2007	Sheet 12 of 41	

DDR Channel A VTT_DDR Decoulping Caps.

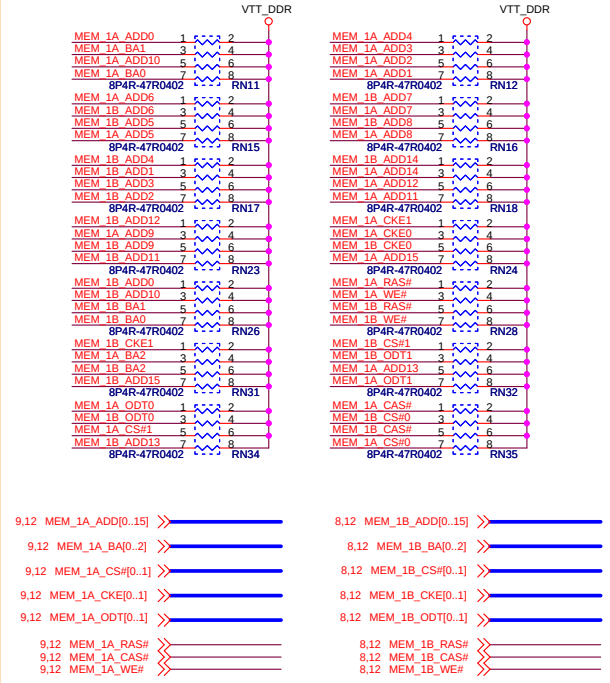
DDR Channel A VCC_DDR Decoulping Caps.



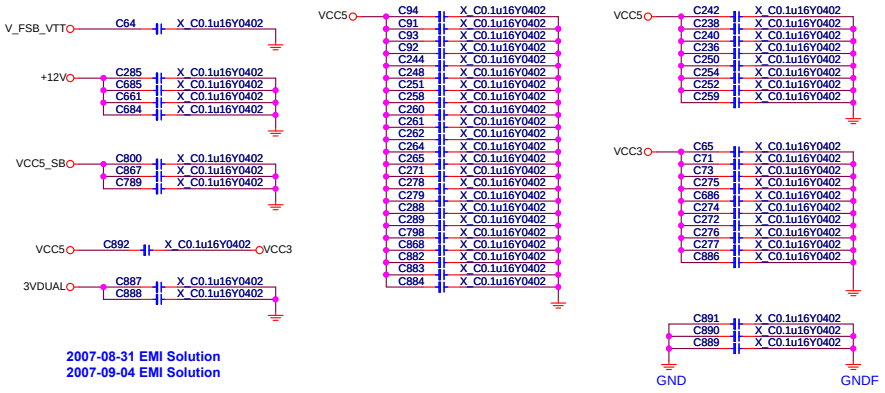
DDR Channel A Termination



DDR Channel B Termination



EMI Solution



2007-08-31 EMI Solution
2007-09-04 EMI Solution

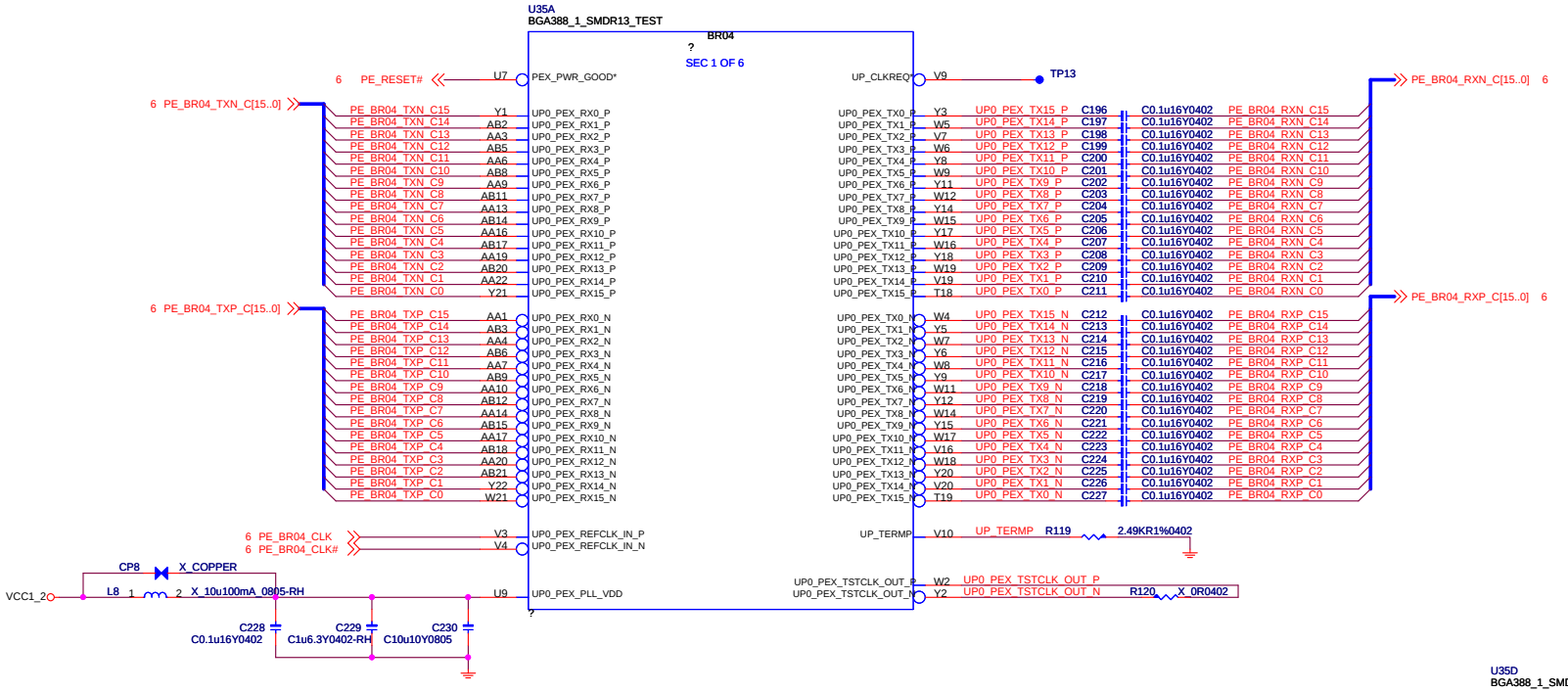
MICRO-START INT'L CO.,LTD.

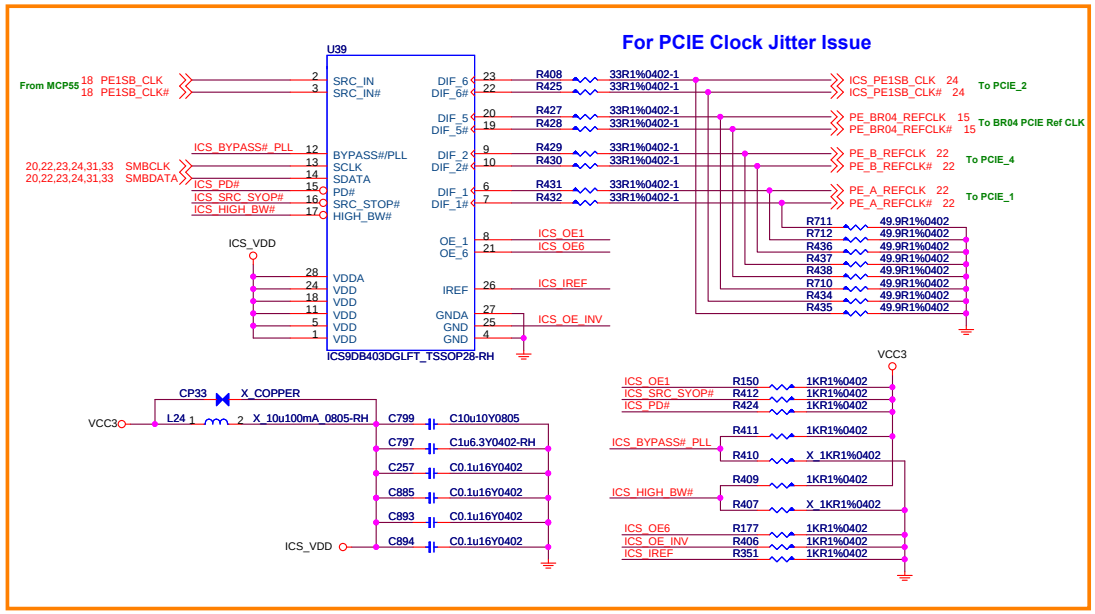
Title: DDR II Termination / EMI

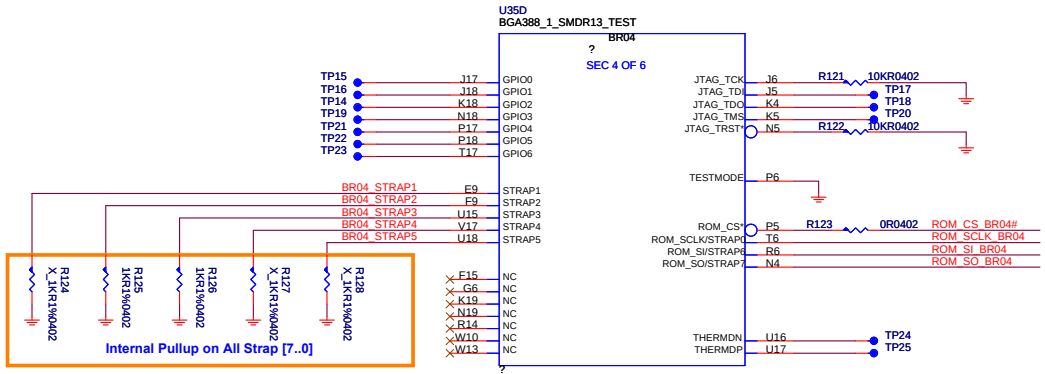
Size	Document Number	Rev
	MS-7510	0A

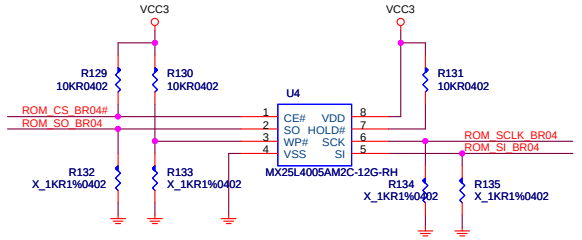
Date: Friday, September 07, 2007 Sheet 13 of 41

C55 to BR04 PCI-Express Interface









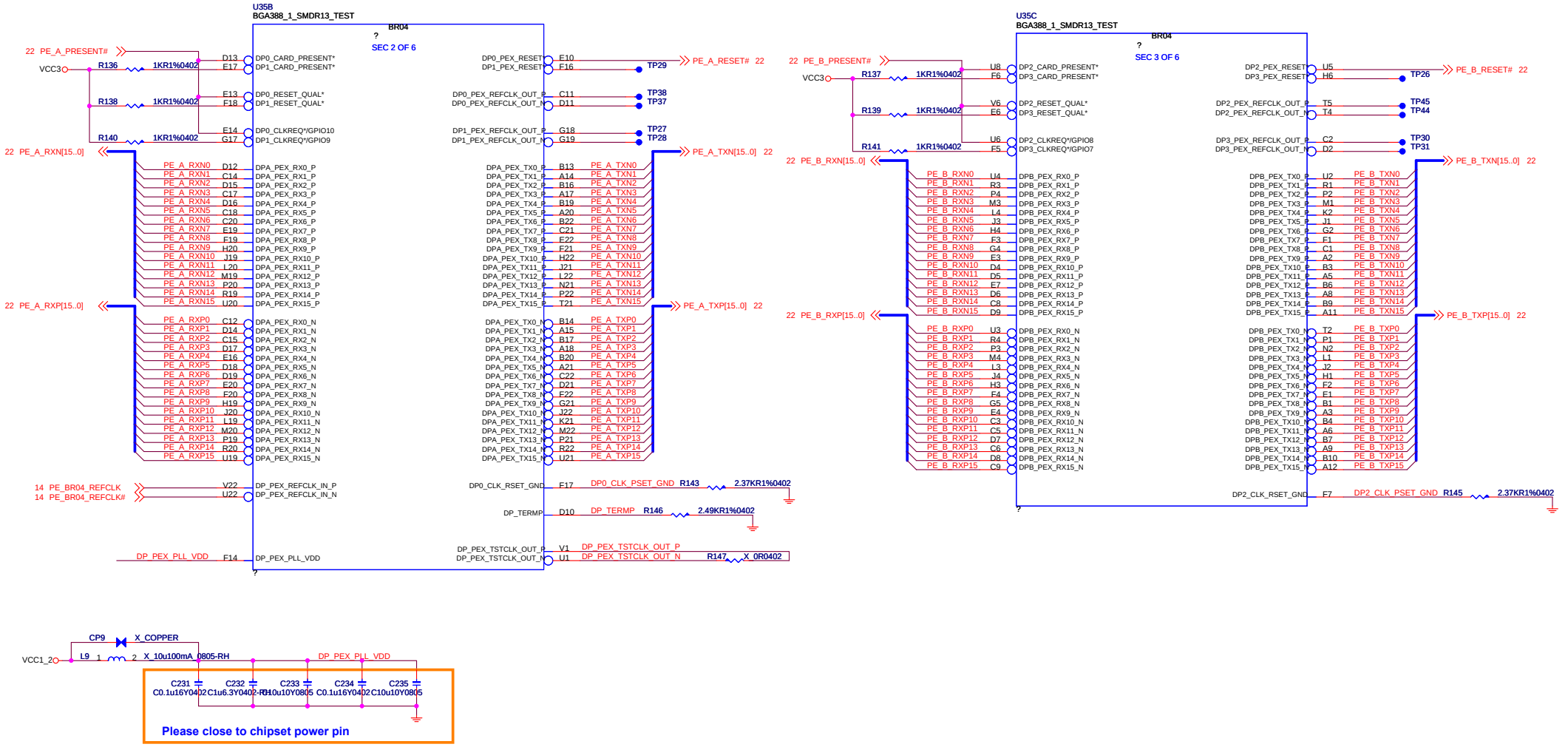
MSI MICRO-START INT'L CO.,LTD.

Title: BR04 - C55 Side

Size	Document Number	Rev
	MS-7510	0A

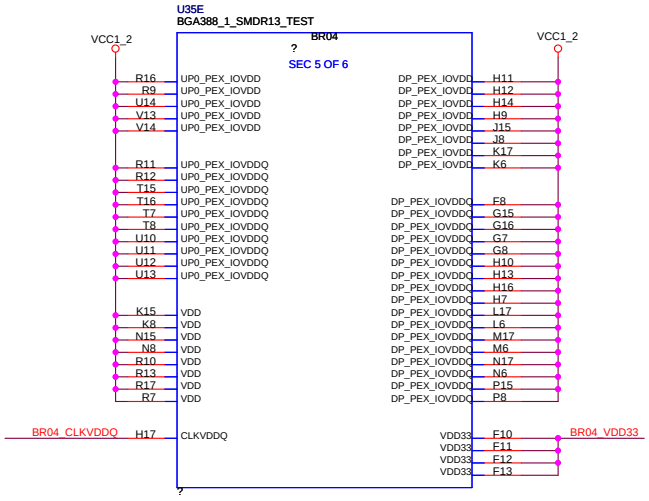
Date: Monday, September 10, 2007 Sheet 14 of 41

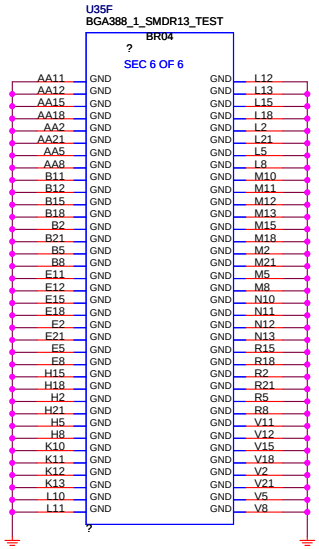
BR04 to PCI-Express Slots

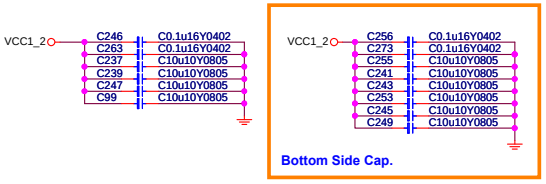


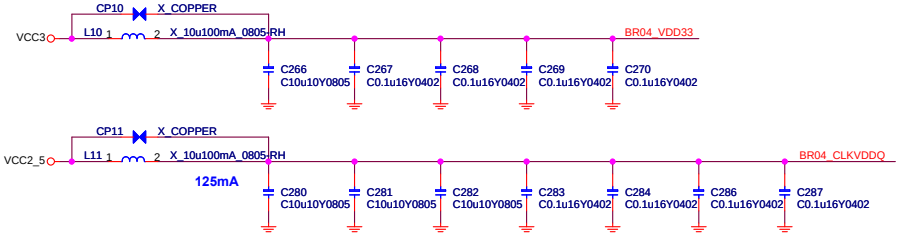
MSI MICRO-START INT'L CO.,LTD.			
Title: BR04 - PCIE x16 Slot			
Size	Document Number: MS-7510		Rev: 0A
Date: Monday, September 10, 2007		Sheet 15 of 41	

BR04 Power and Gnd Block





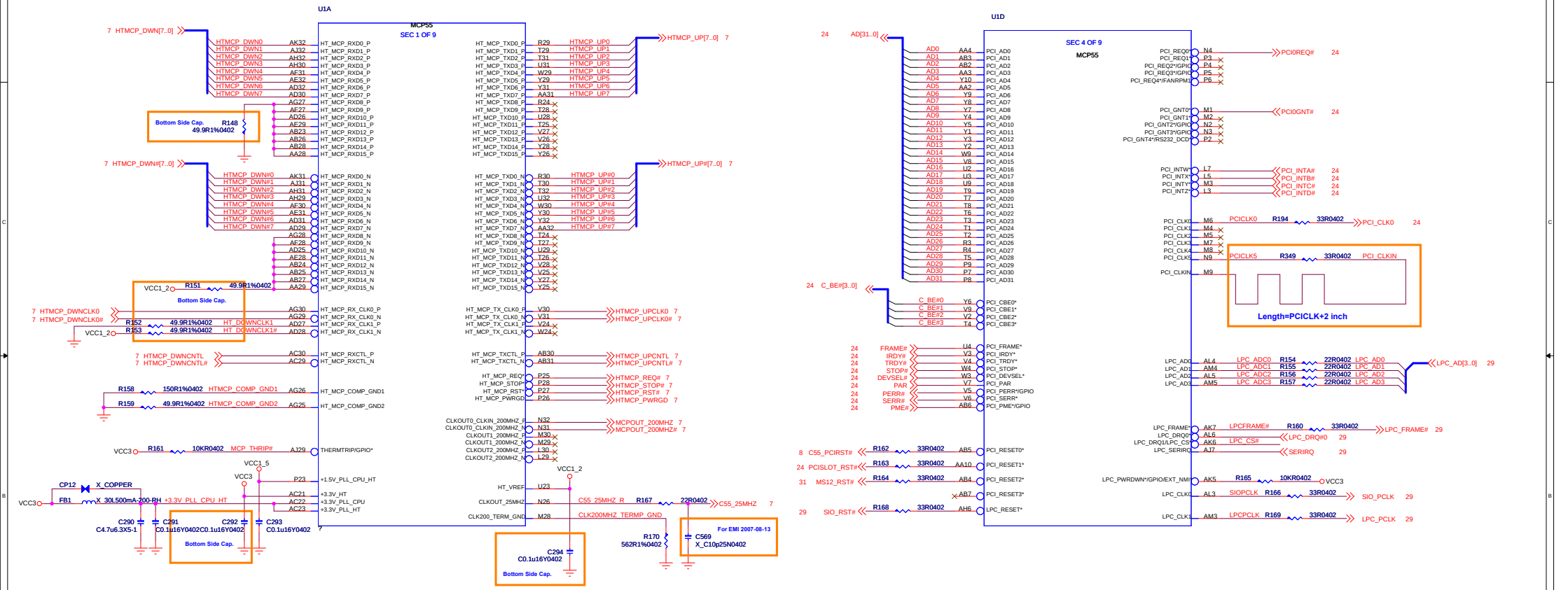


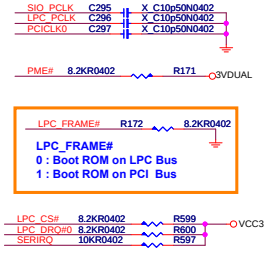


MICRO-START INT'L CO.,LTD.

Title: BR04 - Power / Gnd		
Size	Document Number: MS-7510	Rev: 0A
Date: Friday, September 07, 2007	Sheet 16 of 41	

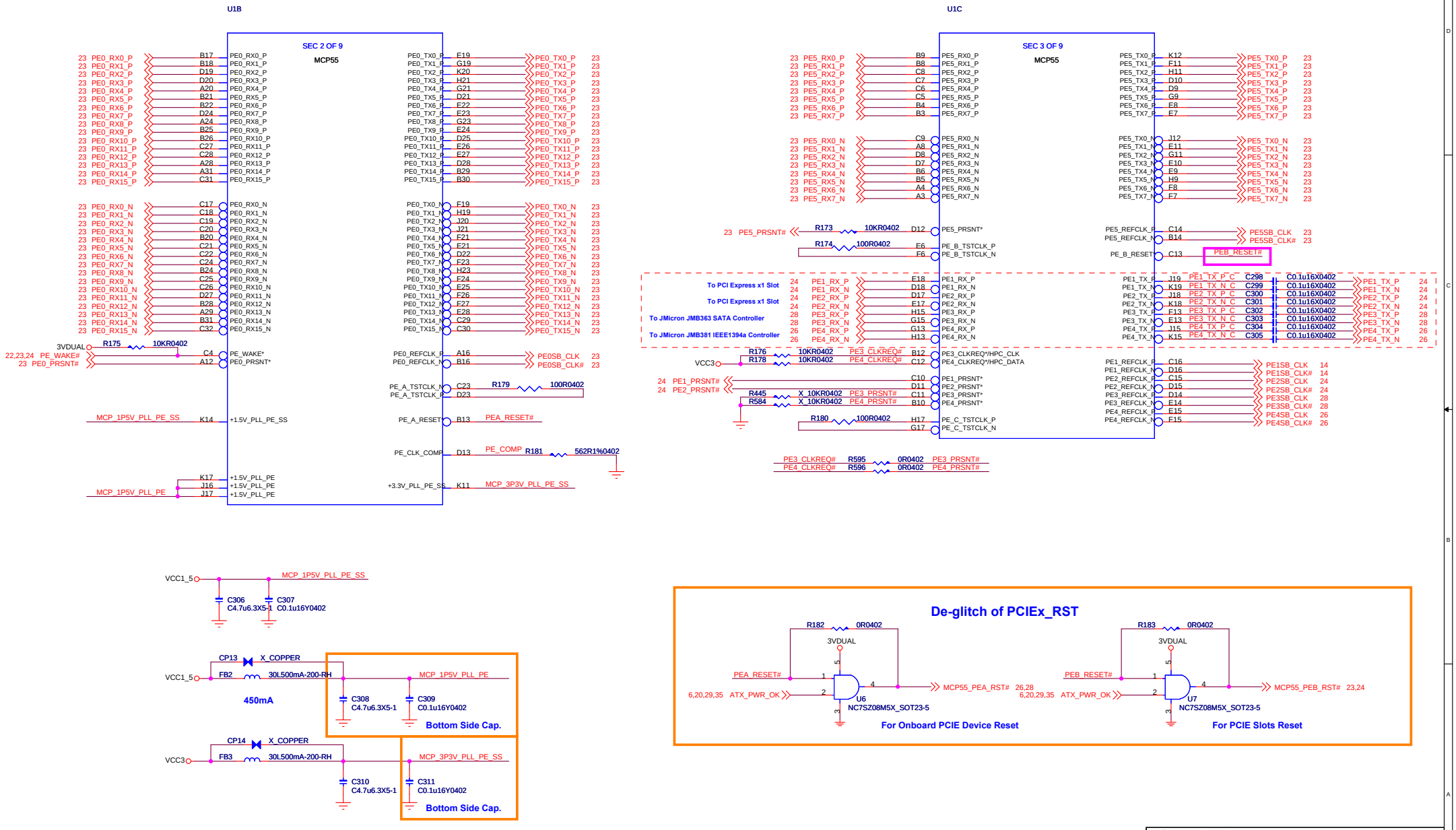
MCP55 - HT / PCI / LPC





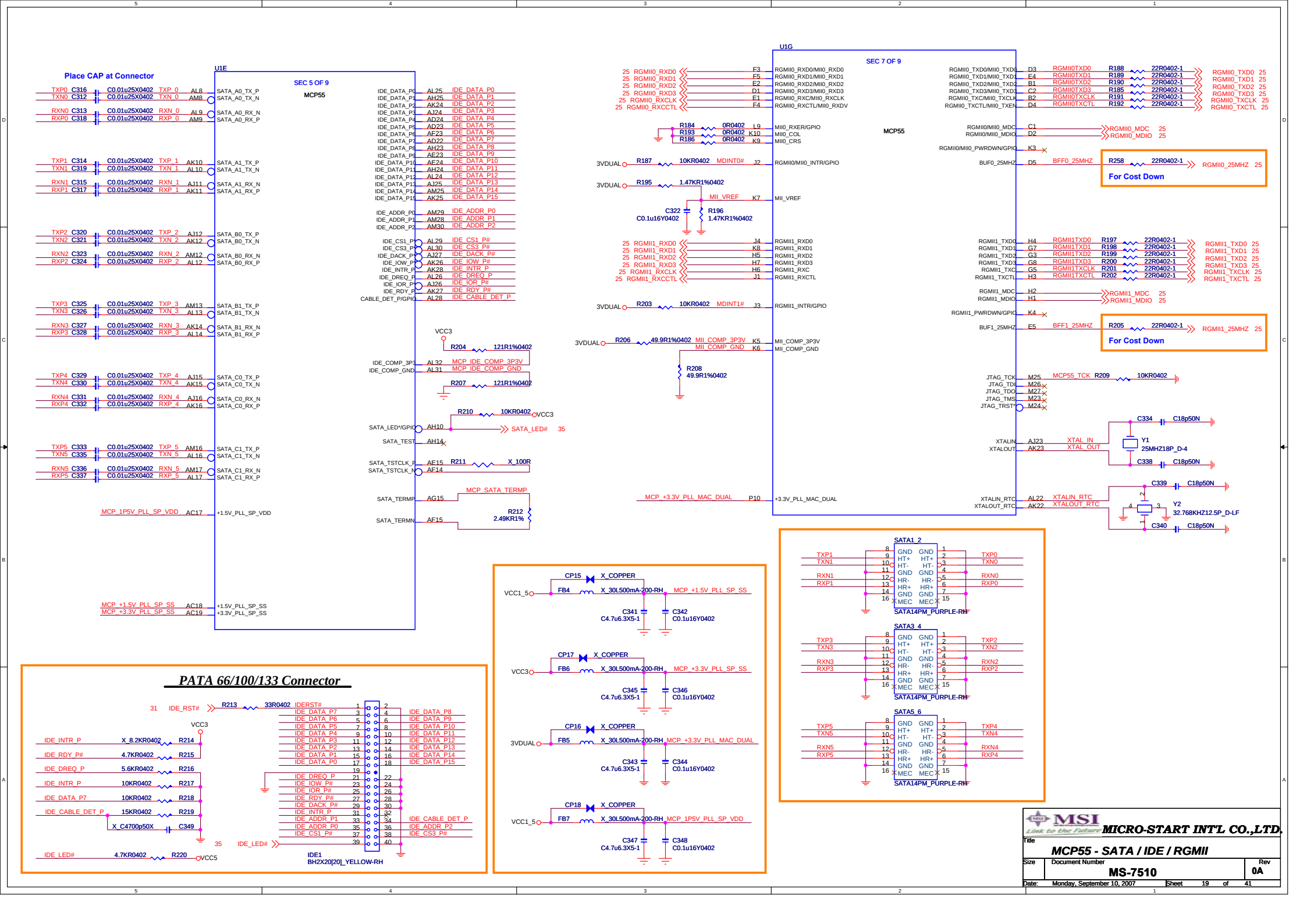
MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	MCP55 - HT / PCI / LPC		
Size	Document Number MS-7510		Rev 0A
Date: Monday, September 10, 2007	Sheet 17 of 41		

MCP55 - PCI-E



MICRO-START INT'L CO.,LTD.

Title	MCP55 - PCI-E	
Size	Document Number: MS-7510	Rev: 0A
Date: Friday, September 07, 2007	Sheet 18 of 41	


Place CAP at Connector
U1E
SEC 5 OF 9
MCP55
U1G
SEC 7 OF 9
MCP55
PATA 66/100/133 Connector
IDE1
BH2X20[20]_YELLOW-RH
SATA1_2
SATA3_4
SATA5_6
SATA14PM_PURPLE-RH
MICRO-START INT'L CO.,LTD.
MCP55 - SATA / IDE / RGMII
MS-7510
0A
Monday, September 10, 2007
Sheet 19 of 41

U1F

SEC 6 OF 9

MCP55

Vcore Power On Sequence Control Circuit

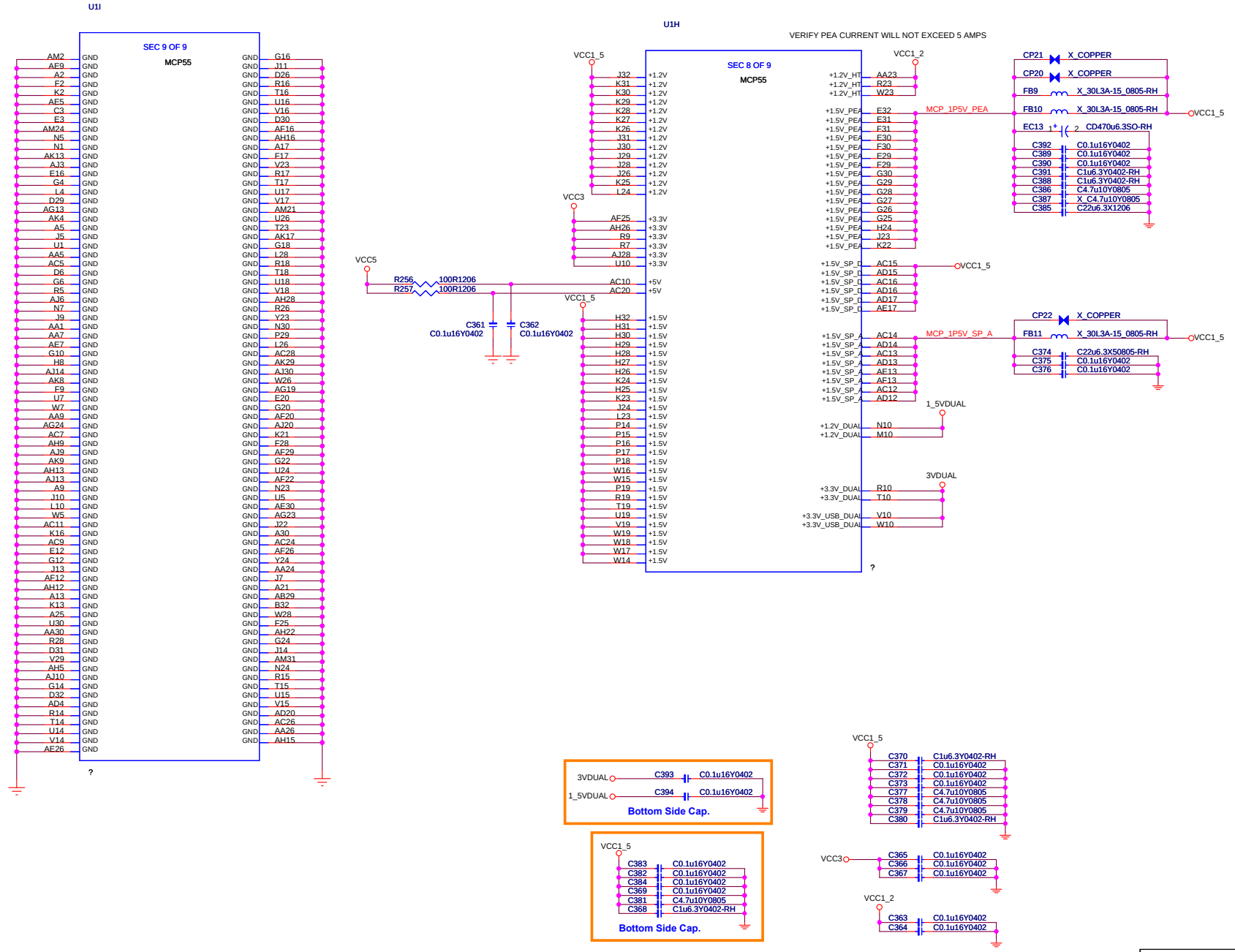
Chasiss Intrusion

SPI EEPROM Clock Speed
00: 50 kHz
01: 99 kHz
10: 480 kHz
11: 893 kHz

Title	MCP55 - Audio / USB / GPIO
Size	Document Number: MS-7510
Rev	0A
Date:	Friday, September 07, 2007
Sheet	20 of 41

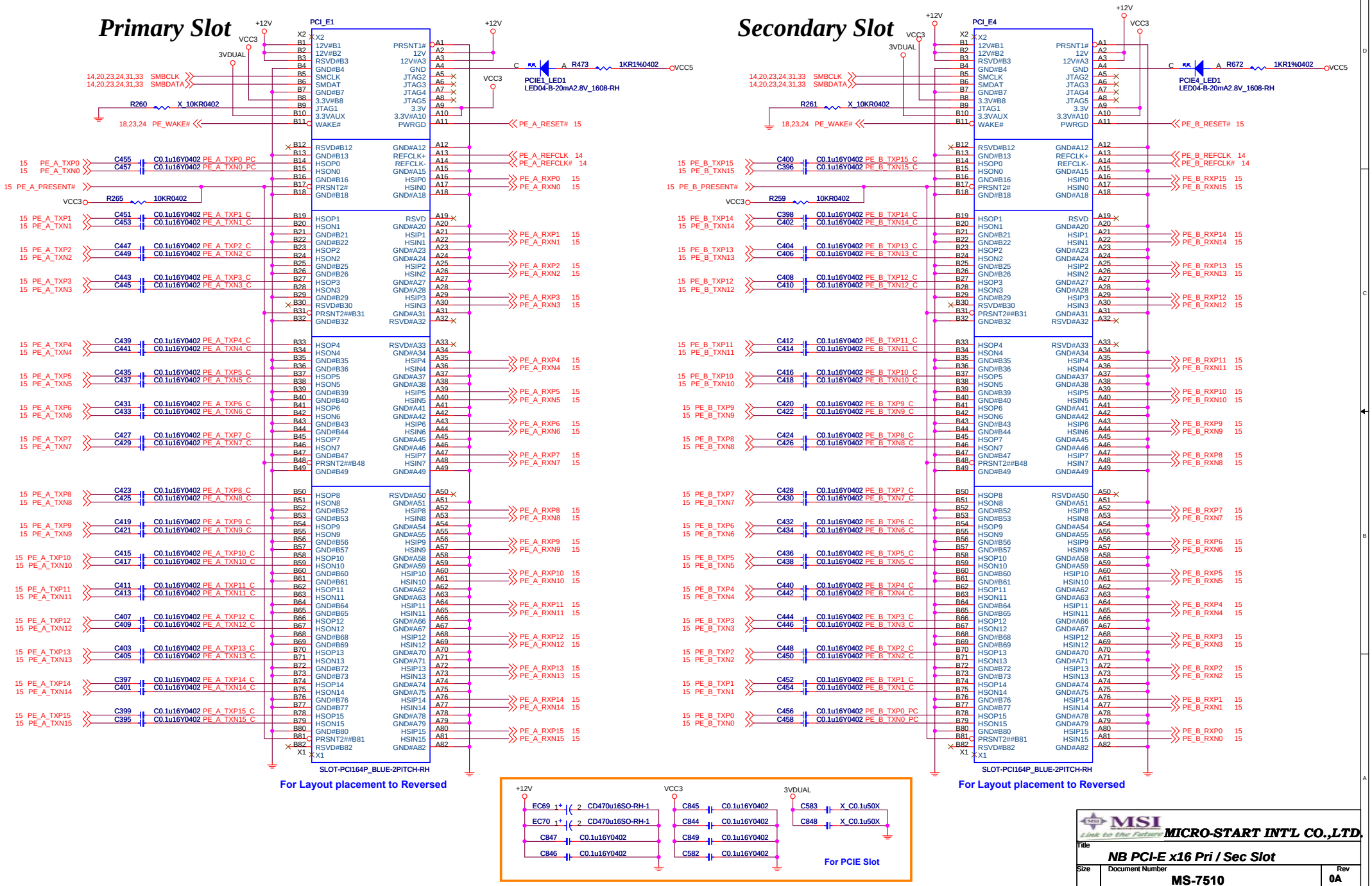
MICRO-START INT'L CO.,LTD.

MCP55 - Power & Gnd



MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title	MCP55 - Power & Gnd	
Size	Document Number MS-7510	Rev 0A
Date: Monday, September 10, 2007	Sheet 21 of 41	

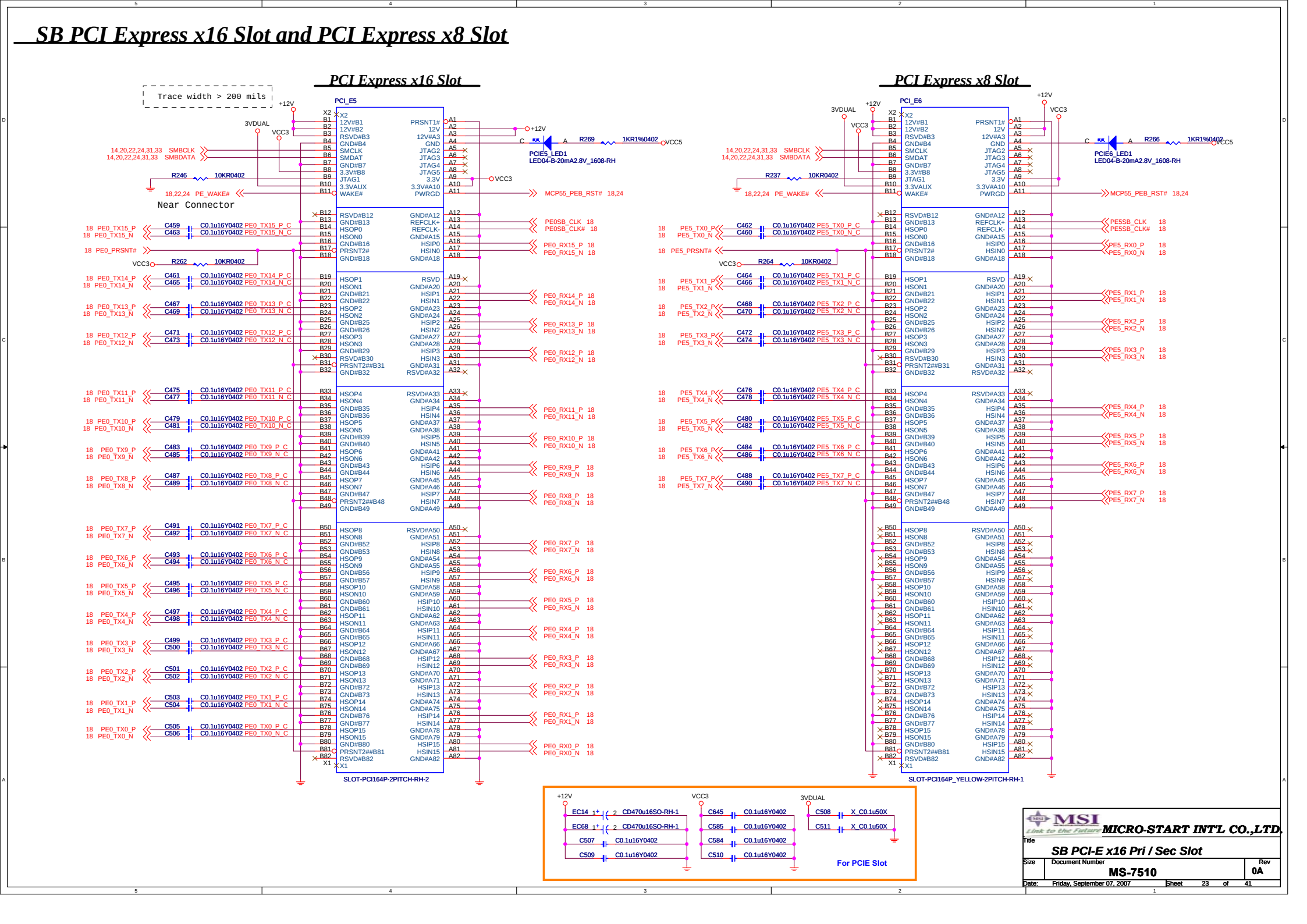
PCI-Express x16 Primary and Secondary Slot



MICRO-START INT'L CO.,LTD.

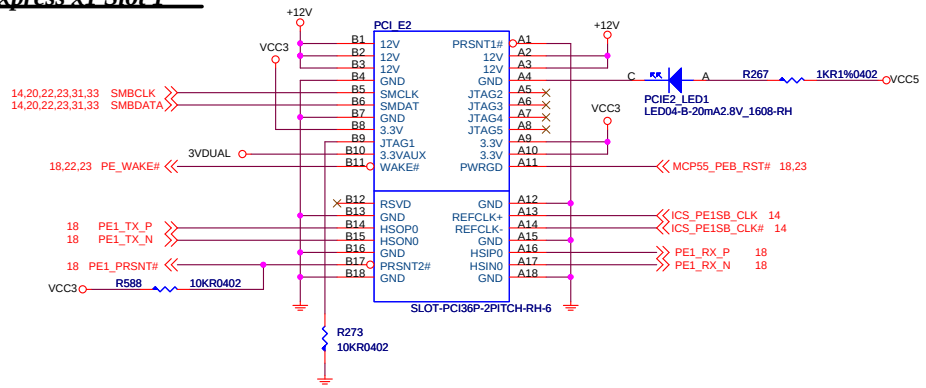
Title	NB PCI-E x16 Pri / Sec Slot	
Size	Document Number: MS-7510	Rev: 0A
Date: Friday, September 07, 2007	Sheet 22 of 41	

SB PCI Express x16 Slot and PCI Express x8 Slot

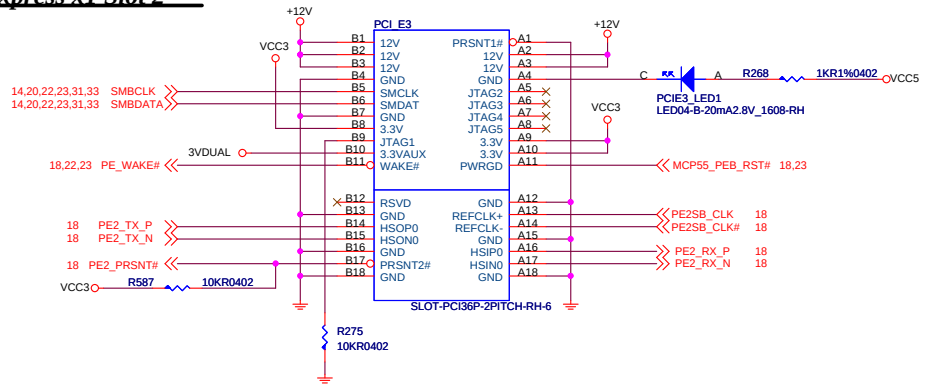


SB PCI-Express x1 Slots and PCI Slot

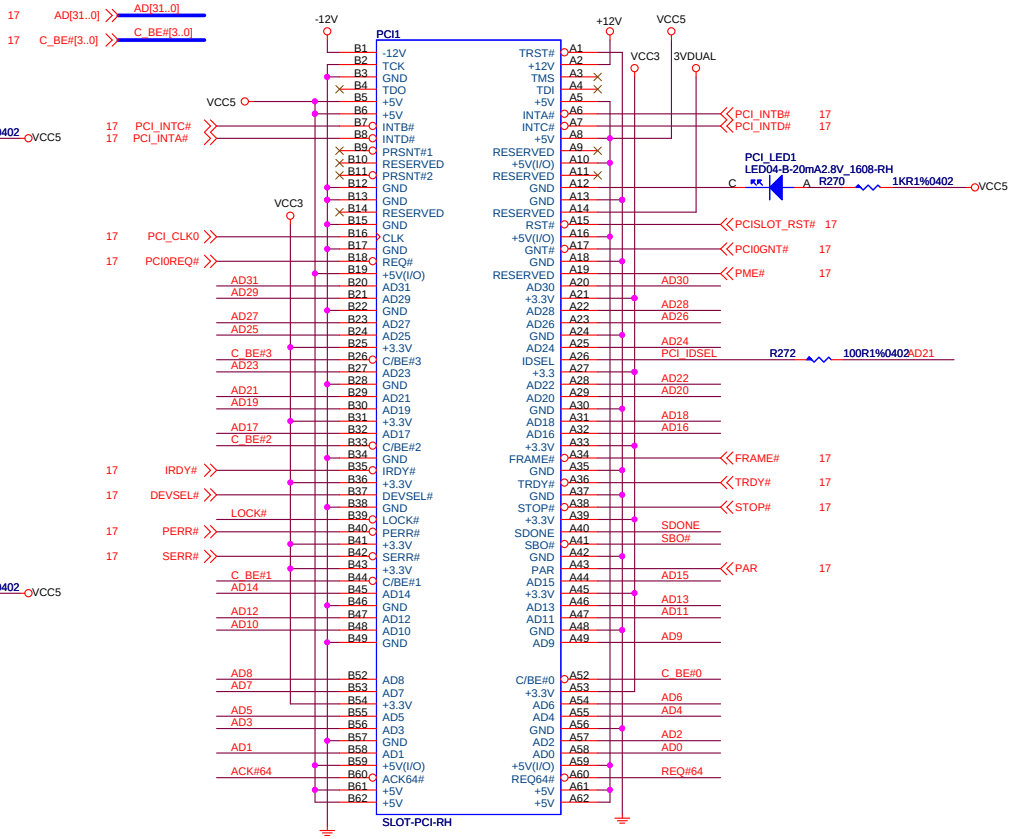
PCI Express x1 Slot 1



PCI Express x1 Slot 2

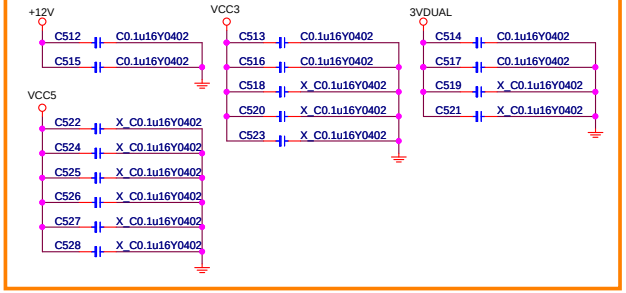


PCI Slot 1 (PCI VER: 2.2 Comply)

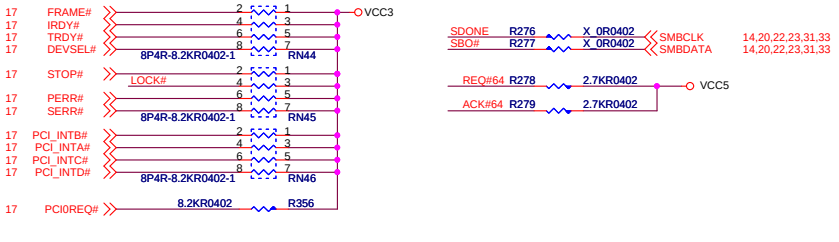


IDSEL = AD21
MASTER = PCI0REQ#
PCI0GNT*

PCI Slot Decoupling Capacitors



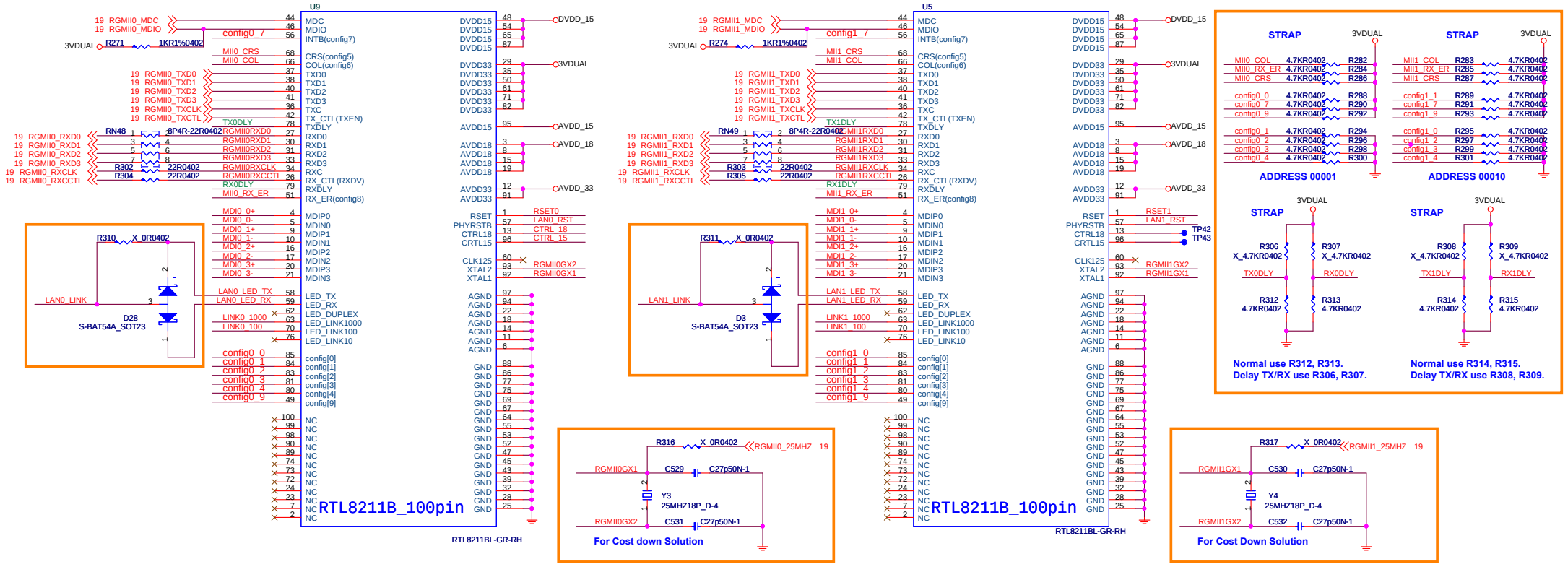
PCI Pull Up / Down Resistors

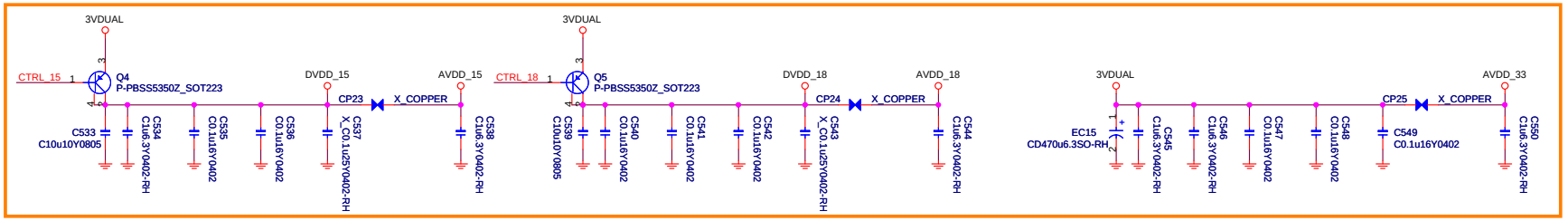


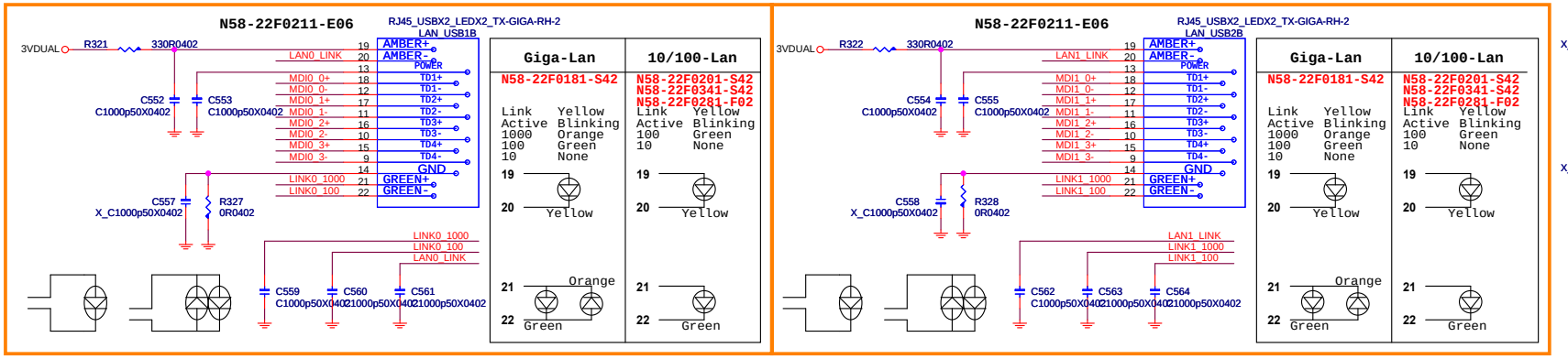
MICRO-START INT'L CO.,LTD.

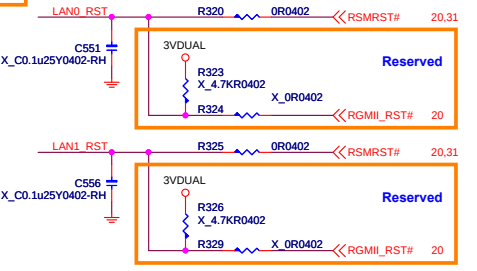
Title	SB PCI-E x1 / PCI Slot	
Size	Document Number MS-7510	Rev 0A
Date: Monday, September 10, 2007	Sheet 24 of 41	

RTL8211B RGMII Gigabit PHY (Lan 1 and Lan 2)





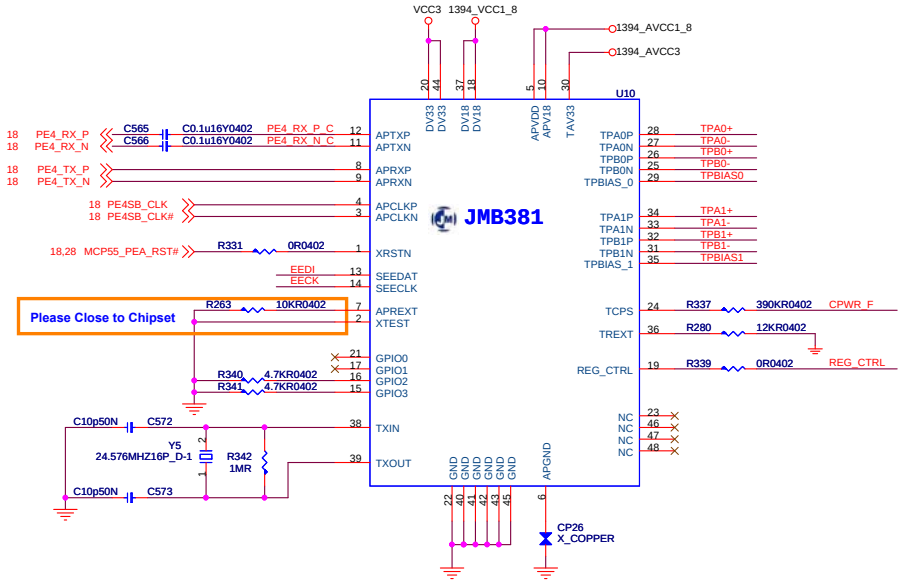


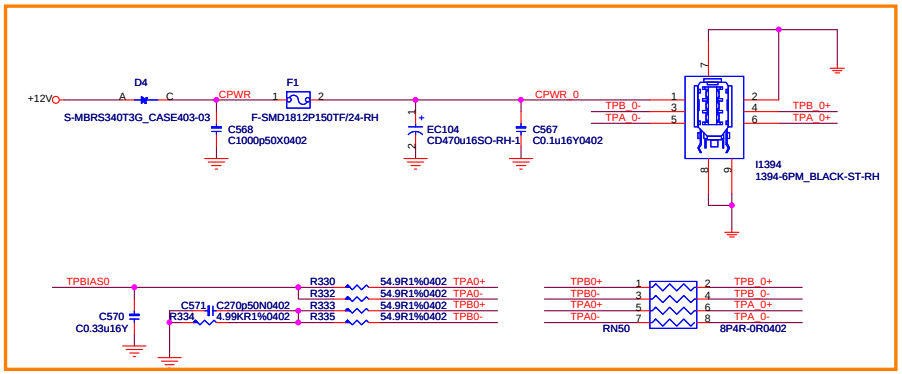


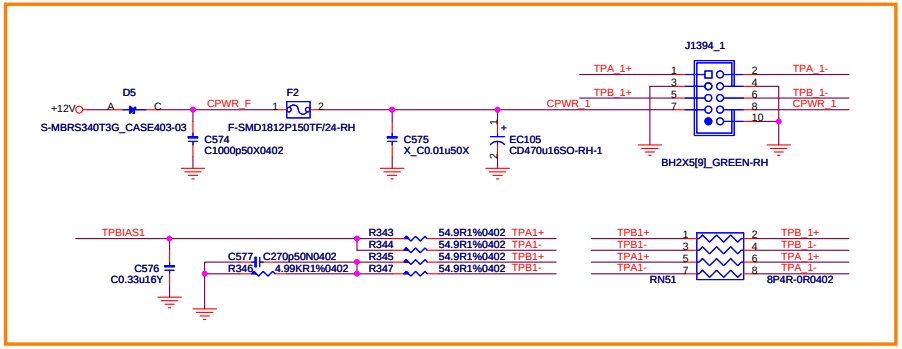
MSI Link to the Future MICRO-START INT'L CO.,LTD.

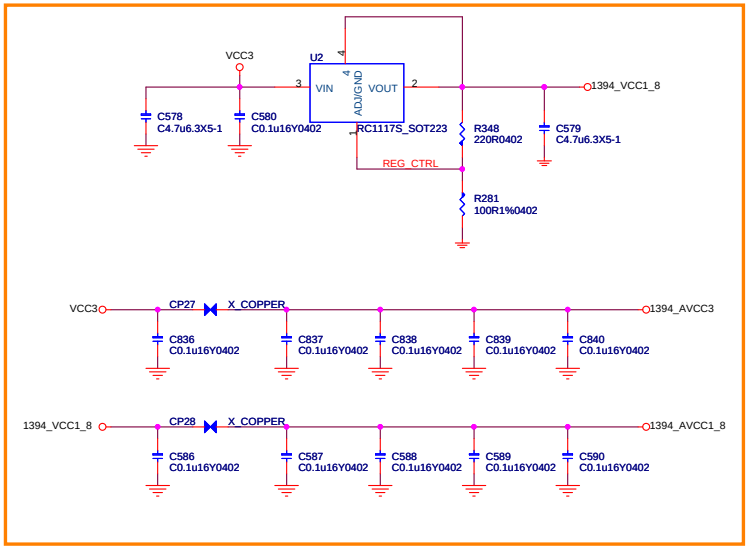
Title	Gigabit PHY - RTL8211B	
Size	Document Number: MS-7510	Rev: 0A
Date: Friday, September 07, 2007	Sheet 25 of 41	

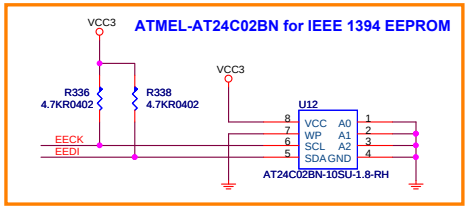
PCIE To 1394a OHCI Host Controller - JMB381







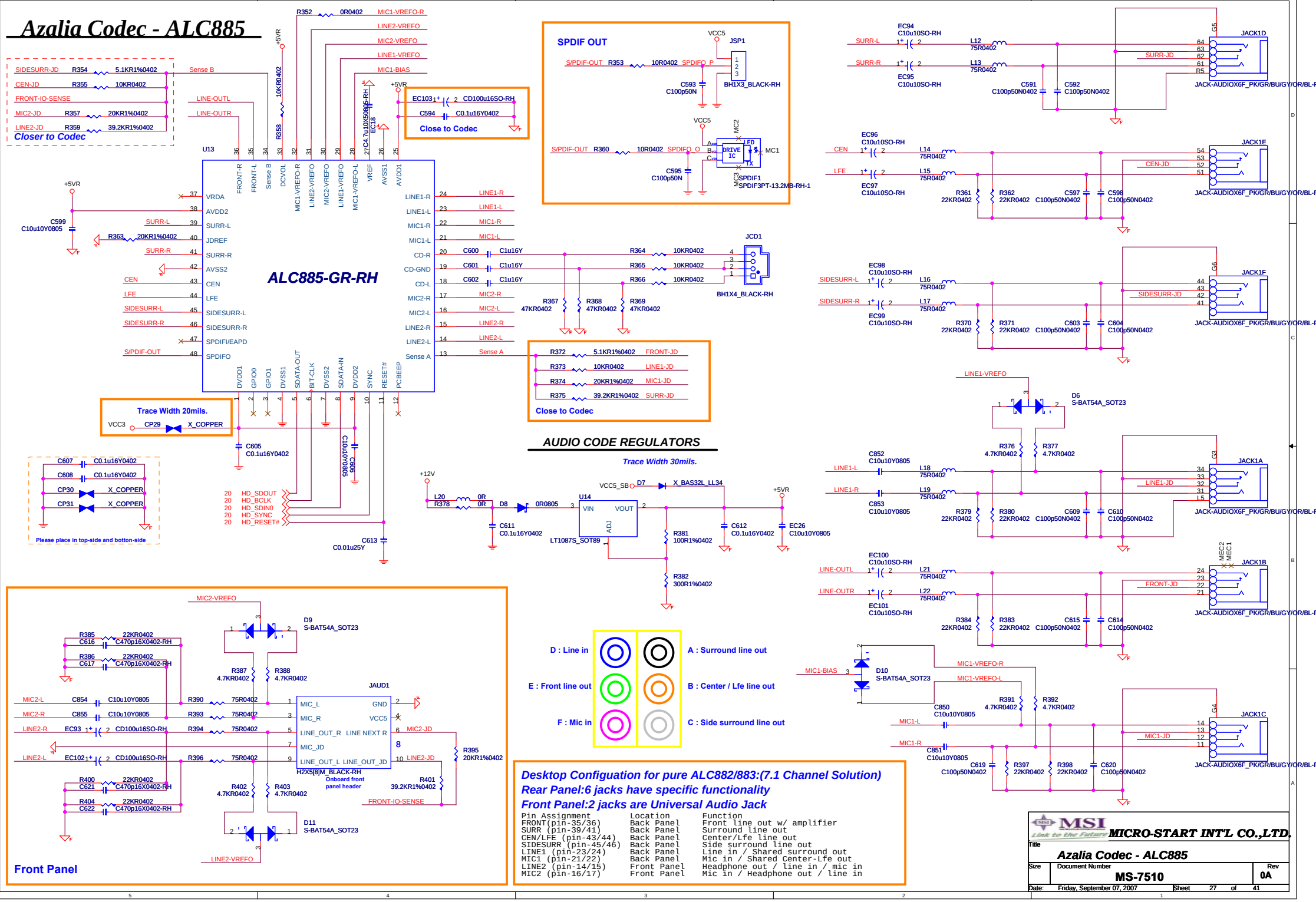




MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	1394 Controller - JMB381	
Size	Document Number MS-7510	Rev 0A
Date: Friday, September 07, 2007	Sheet 26 of 41	

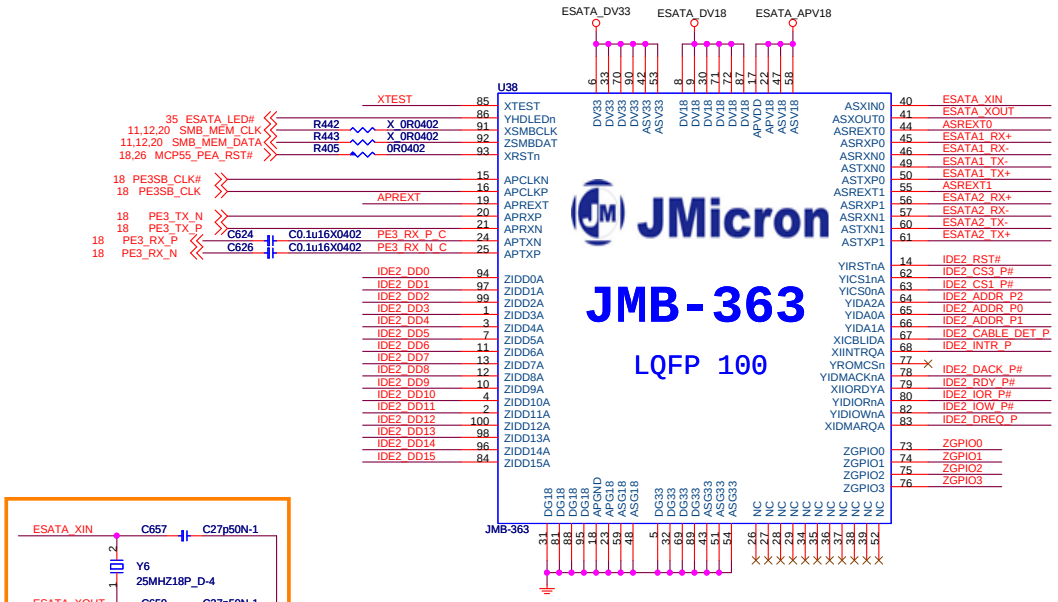
Azalia Codec - ALC885

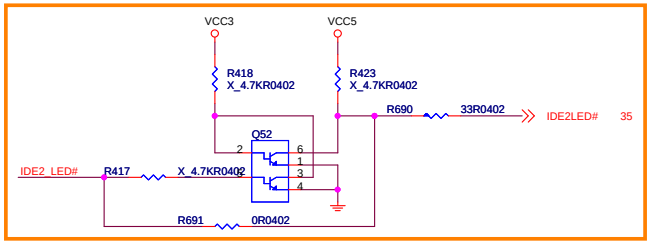


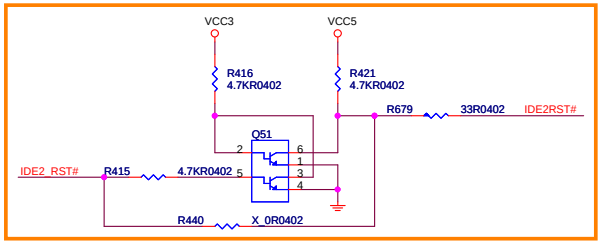
MICRO-START INT'L CO.,LTD.

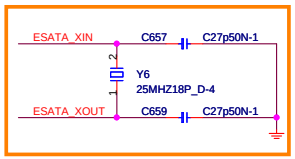
Title	Azalia Codec - ALC885	
Size	Document Number MS-7510	Rev 0A
Date: Friday, September 07, 2007	Sheet 27 of 41	

JMicron JMB363 eSATA Controller





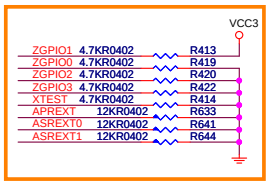


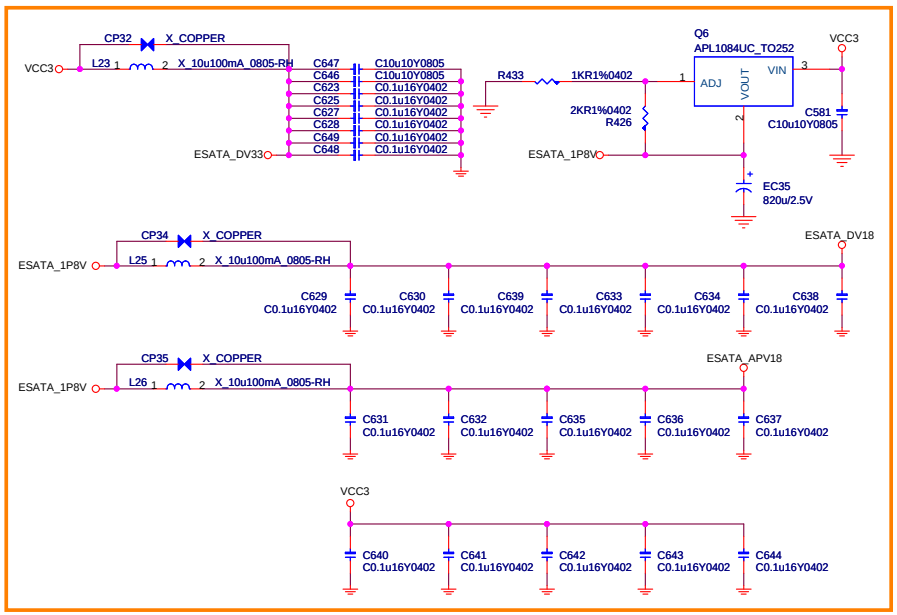


SATA II Port 0 External Reference Resistor.
An external 12KΩ±1%resistor should be connected and bypass to the ground ASG18 (pin#48).

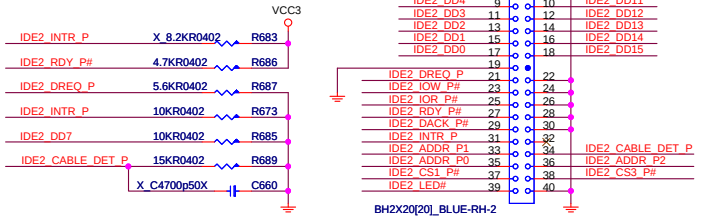
SATA II Port 0 External Reference Resistor.
An external 12KΩ±1%resistor should be connected and bypass to the ground ASG18 (pin#59).

PCI Express External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground APG18 (pin#18).

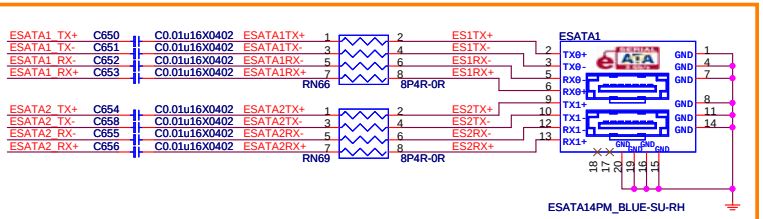




PATA 66/100/133 Connector



JMB363 GPIO0
It uses to control function# available on JMB363.
0: single function ; 1: multi-function
JMB363 GPIO1
It uses to control clock source of SATA II port 0.
0: from internal clock source from PCI Express clock source
1: from ASXIN0 & ASXOUT0
JMB363 GPIO2
It uses to control interface to access internal debug registers.
0: SMBus I/F ; 1: Reserved for debugging.
JMB363 GPIO3
Reserved for debugging.
JMB363 Test Mode Enable.
High-active signal to enable testing and debug modes of JMB363.



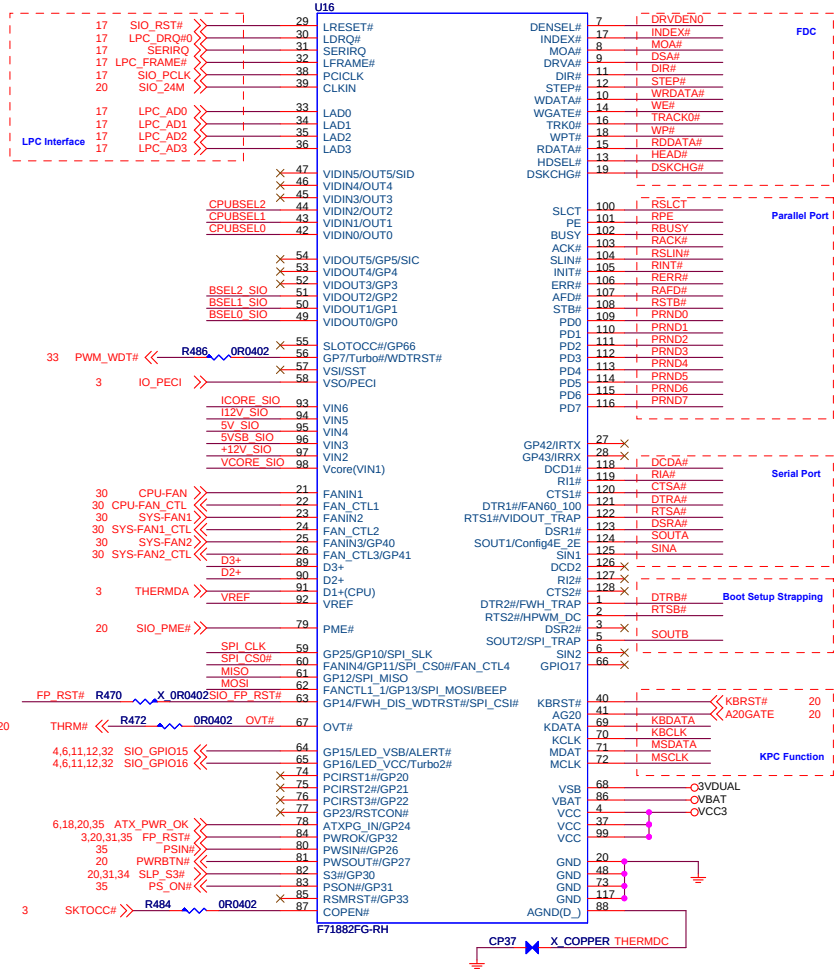
MICRO-START INT'L CO.,LTD.

Title: JMicron JMB363 eSATA Controller

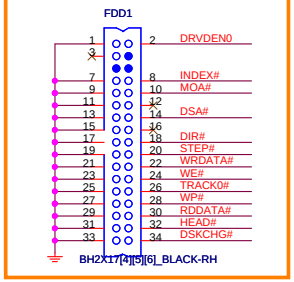
Size	Document Number	Rev
	MS-7510	0A

Date: Monday, September 10, 2007 Sheet 28 of 41

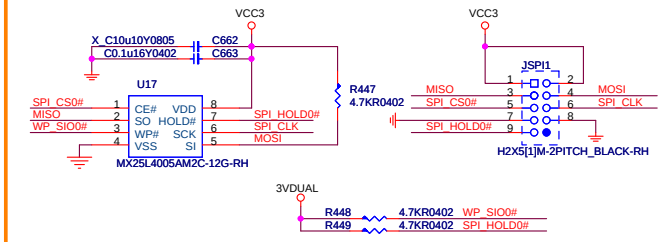
Super I/O FinTek F71882FG



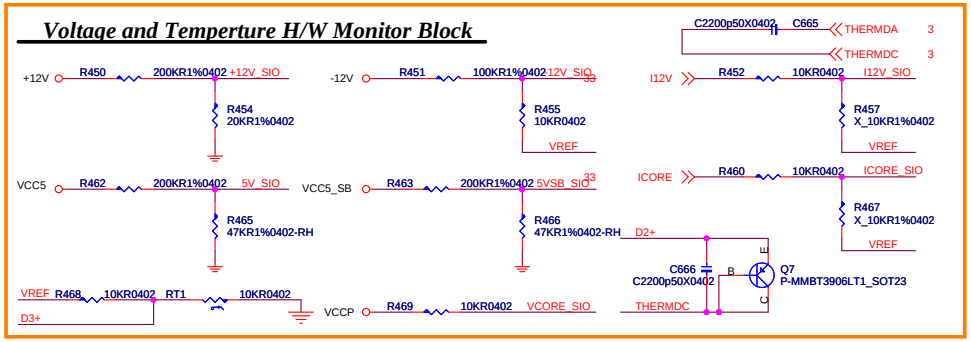
Floppy Connector



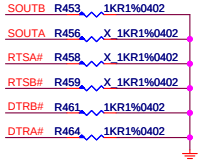
SPI Flash ROM and Debug Port



Voltage and Temperture H/W Monitor Block

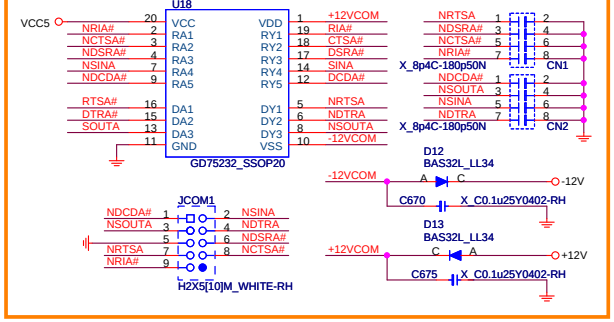


Boot Setup Strapping

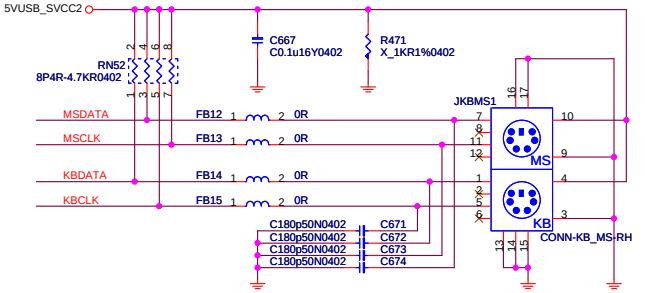


	Don't Stuff	Stuff
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRB#,SOUTB	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN Start Duty 60%	FAN Start Duty 100%

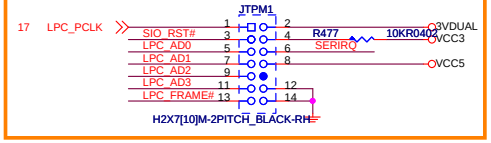
Serial Port (COM1)



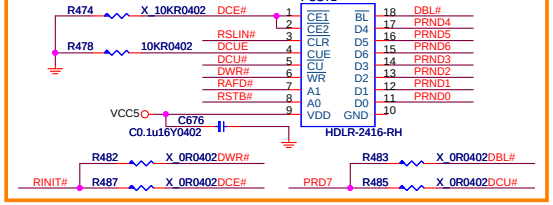
PS2 Keyboard and Mouse Connector



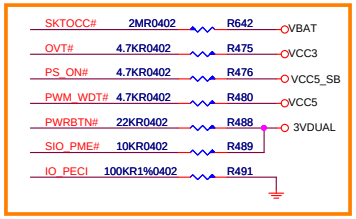
TPM Module Port

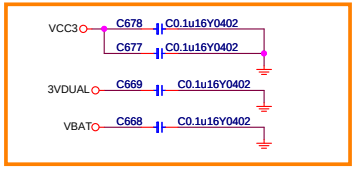


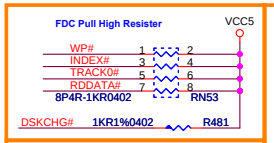
Debug LED Port

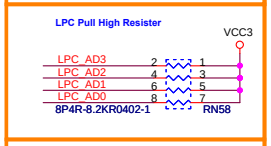


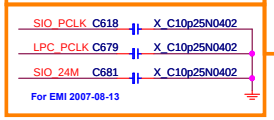
Pull-up / Pull-down Resistors

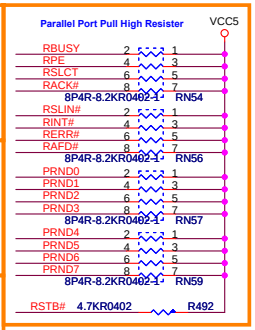


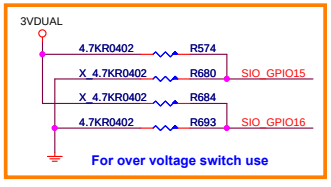


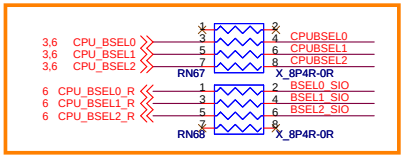










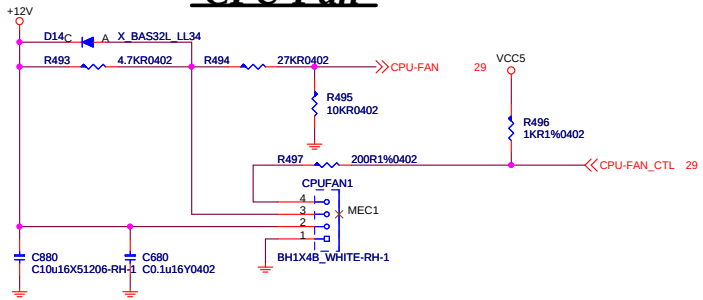


MSI — Link to the Future — MICRO-START INT'L CO.,LTD.

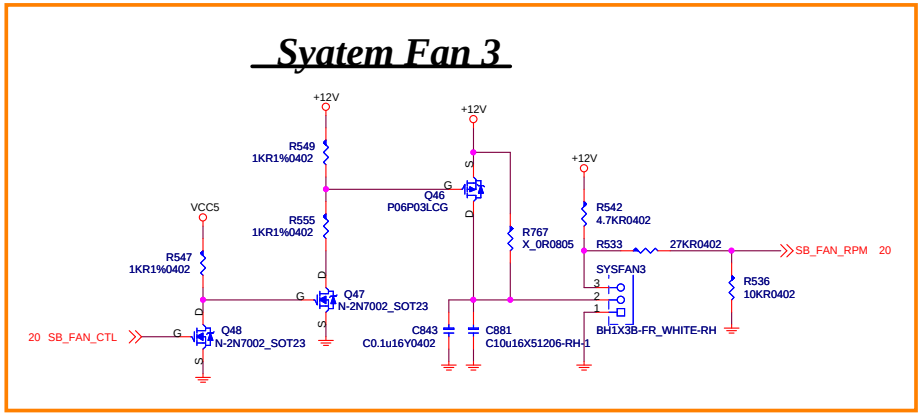
Title	Super I/O - F71882FG	
Size	Document Number: MS-7510	Rev: 0A
Date: Monday, September 10, 2007	Sheet 29 of 41	

Fan Controller

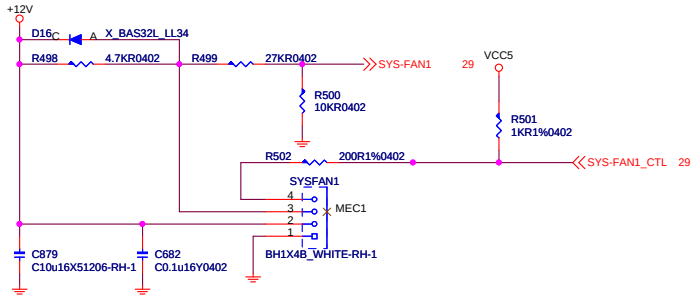
CPU Fan



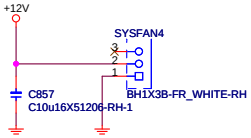
Syatem Fan 3



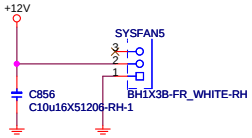
System Fan 1



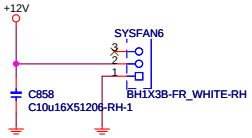
System Fan 4



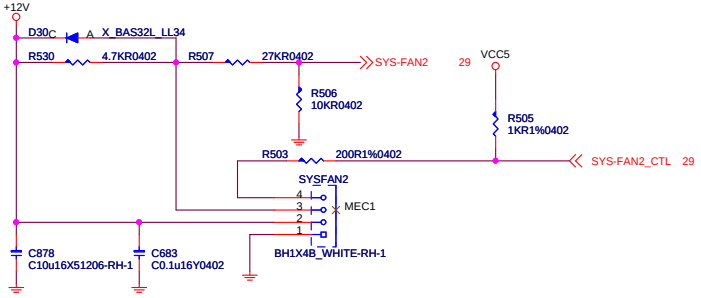
System Fan 5



System Fan 6



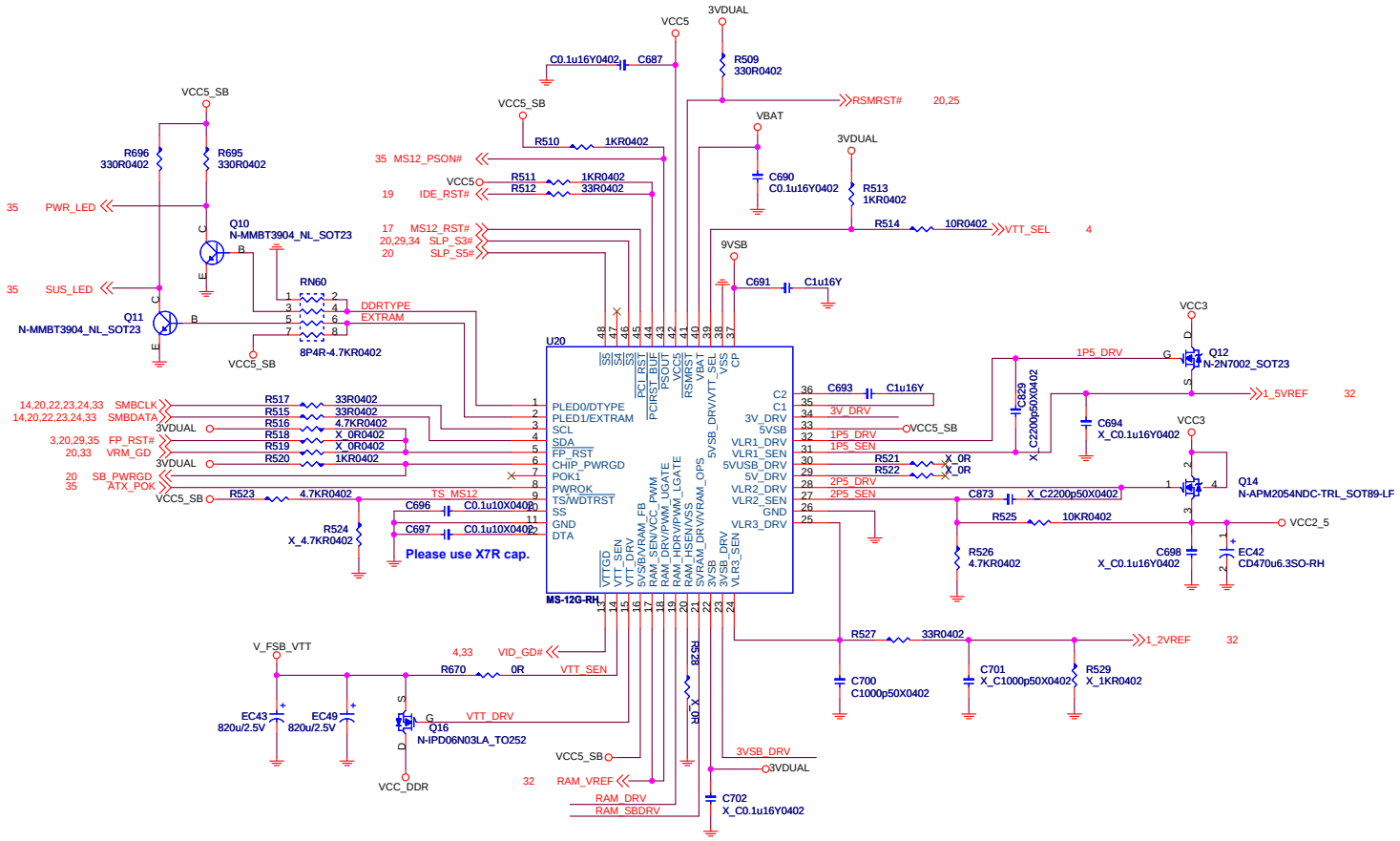
System Fan 2



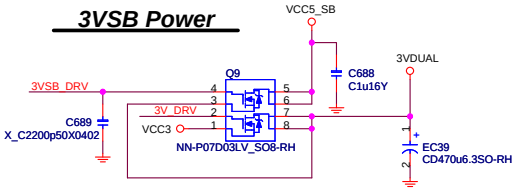
MICRO-START INT'L CO.,LTD.

Title: Fan Controller		
Size	Document Number: MS-7510	Rev: 0A
Date: Monday, September 10, 2007	Sheet 30 of 41	

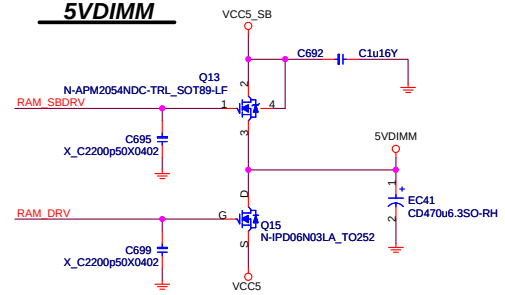
MS12 ACPI Controller

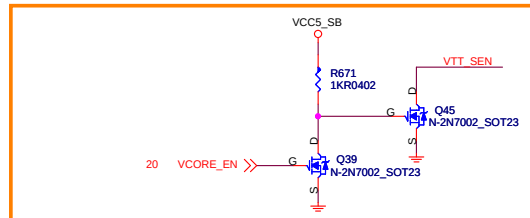


3VSB Power

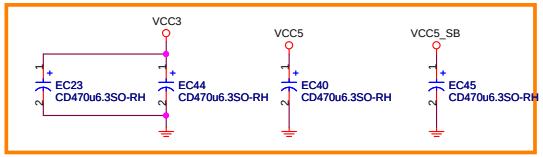


5VDIMM



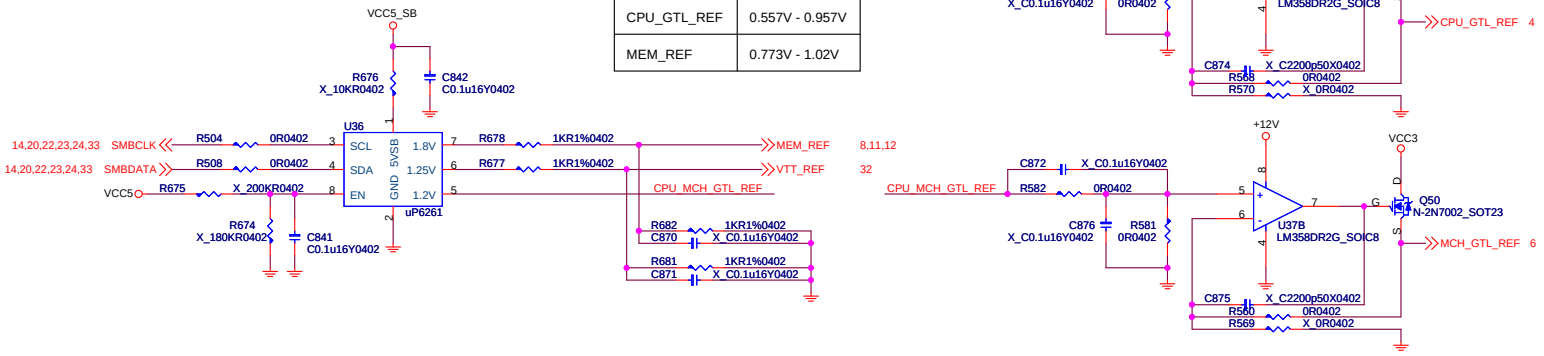


FSB_VTT Power On Sequence Control Circuit



Over Voltage Block

	Voltage Range
DDR_VTT	0.7V - 1.1V
CPU_GTL_REF	0.557V - 0.957V
MEM_REF	0.773V - 1.02V



PIN	PIN INTRODUCTION	
1	PLED0/DDRTYPE	DDRTYPE 0: DDR3(1.5V) 1: DDR2(1.8V)
2	PLED1/EXTRAM	EXTRAM 0: LINEAR MODE 1: PWM MODE
9	TS_MS7	TS_MS7: 0: MS12 Timing 1: MS7 Timing
39	VTT_SEL	VTT_SEL (Pin-39) 0: VTT=1.1V 1: VTT=1.2V

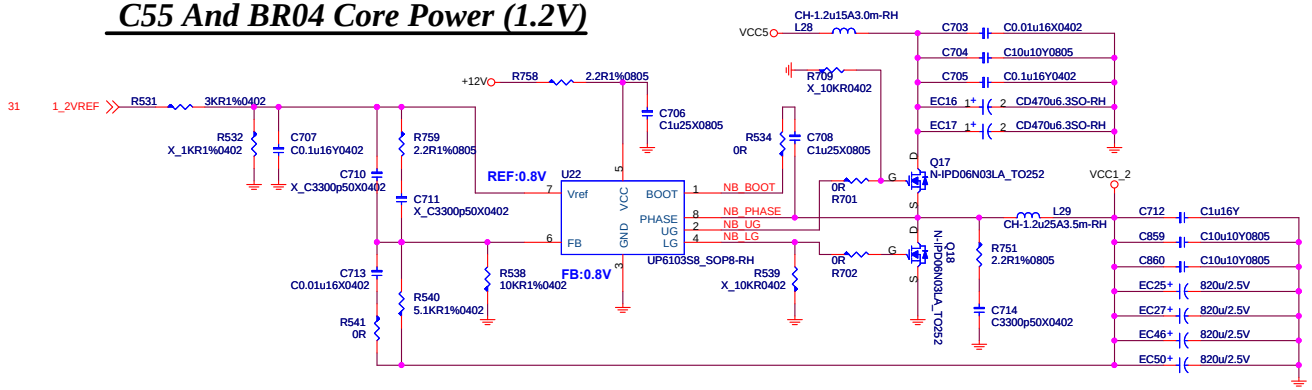
MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: **MS12 ACPI Controller**

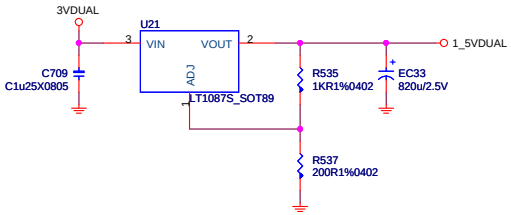
Size	Document Number	Rev
	MS-7510	0A

Date: Monday, September 10, 2007 Sheet 31 of 41

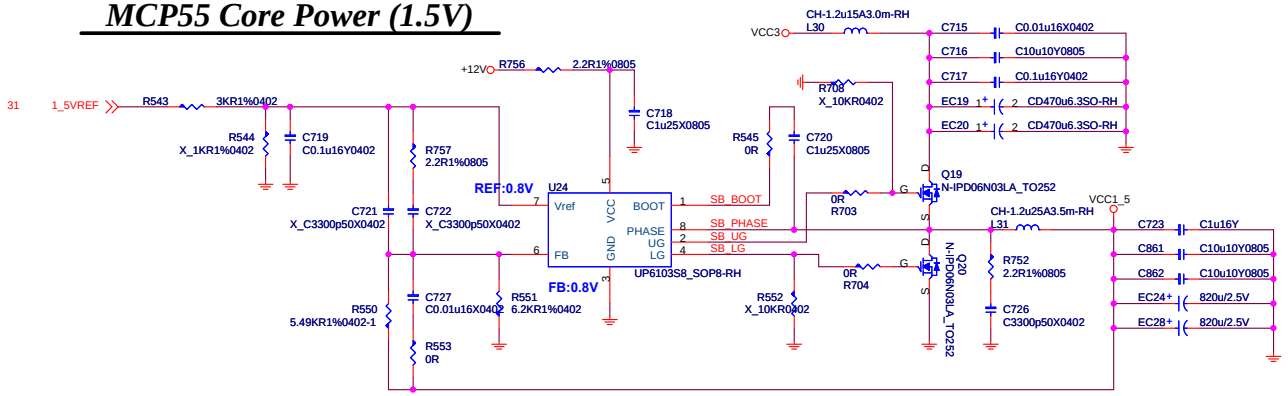
C55 And BR04 Core Power (1.2V)



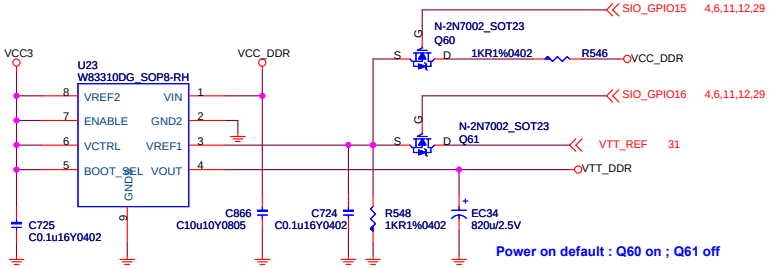
MCP55 1.5V Dual Power (1.5V)



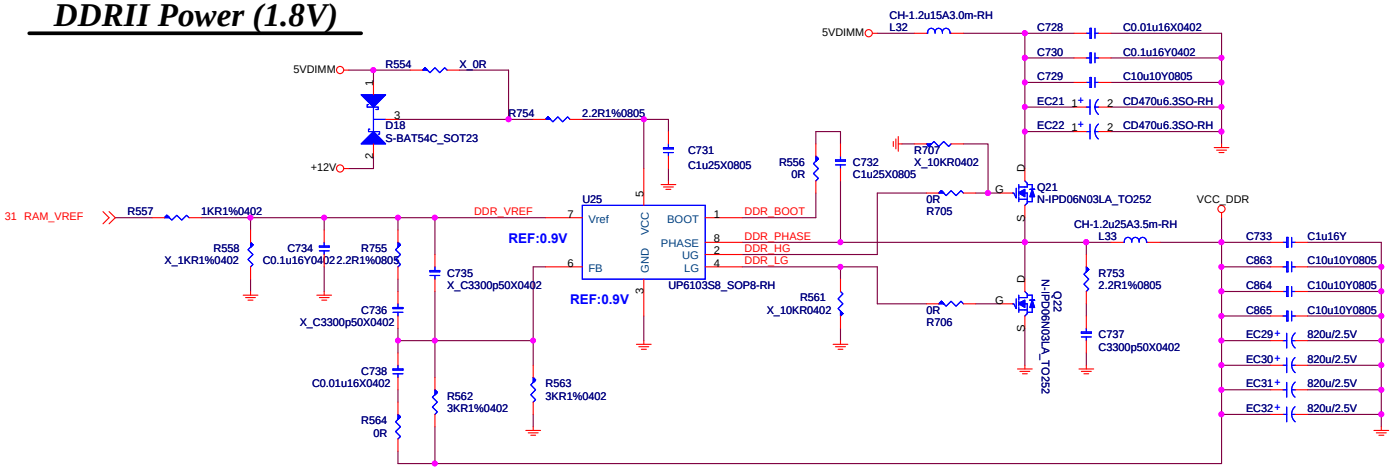
MCP55 Core Power (1.5V)



DDR VTT Power (0.9V)



DDRII Power (1.8V)



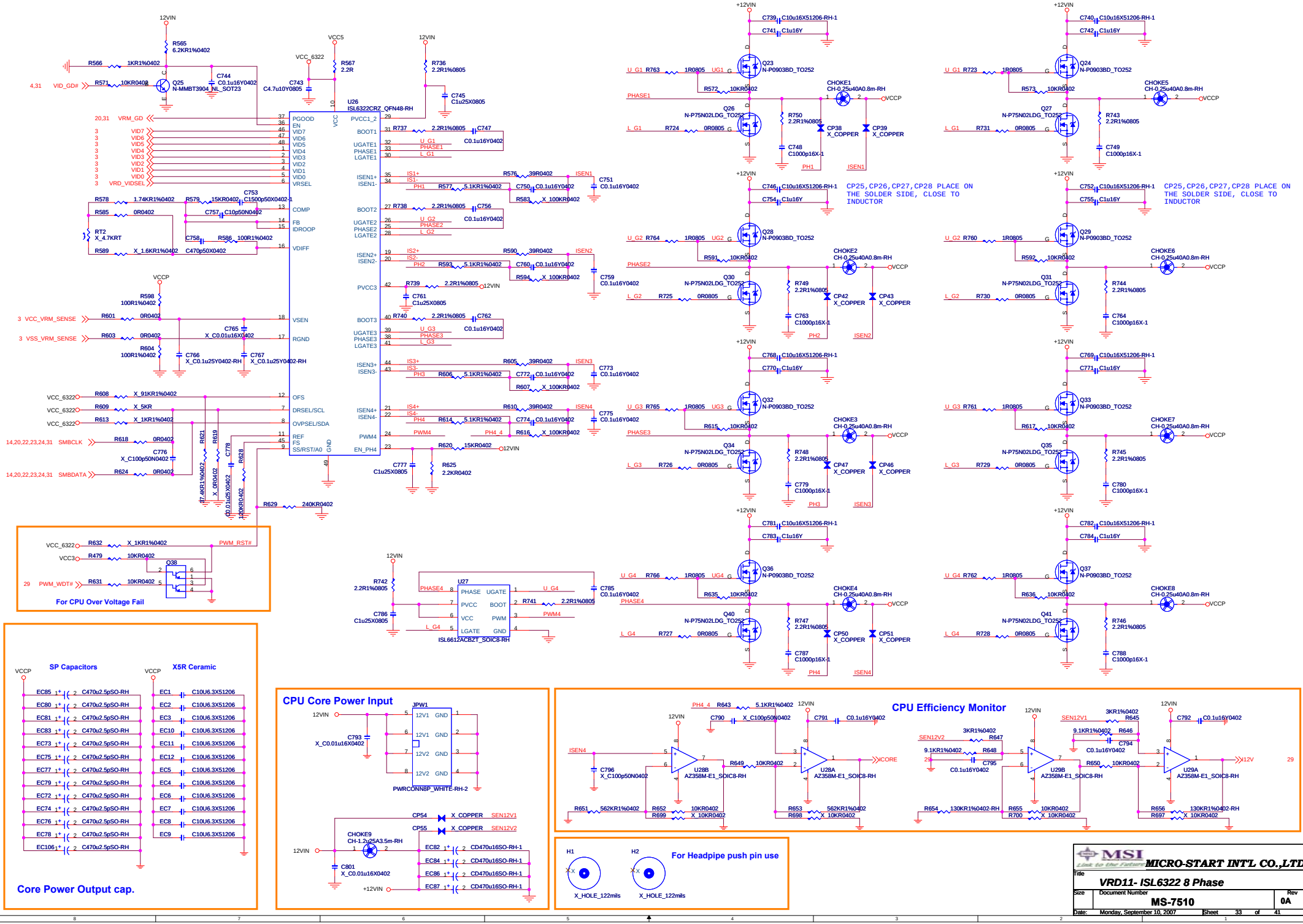
MICRO-START INT'L CO.,LTD.

Title: uPI Power Regulator

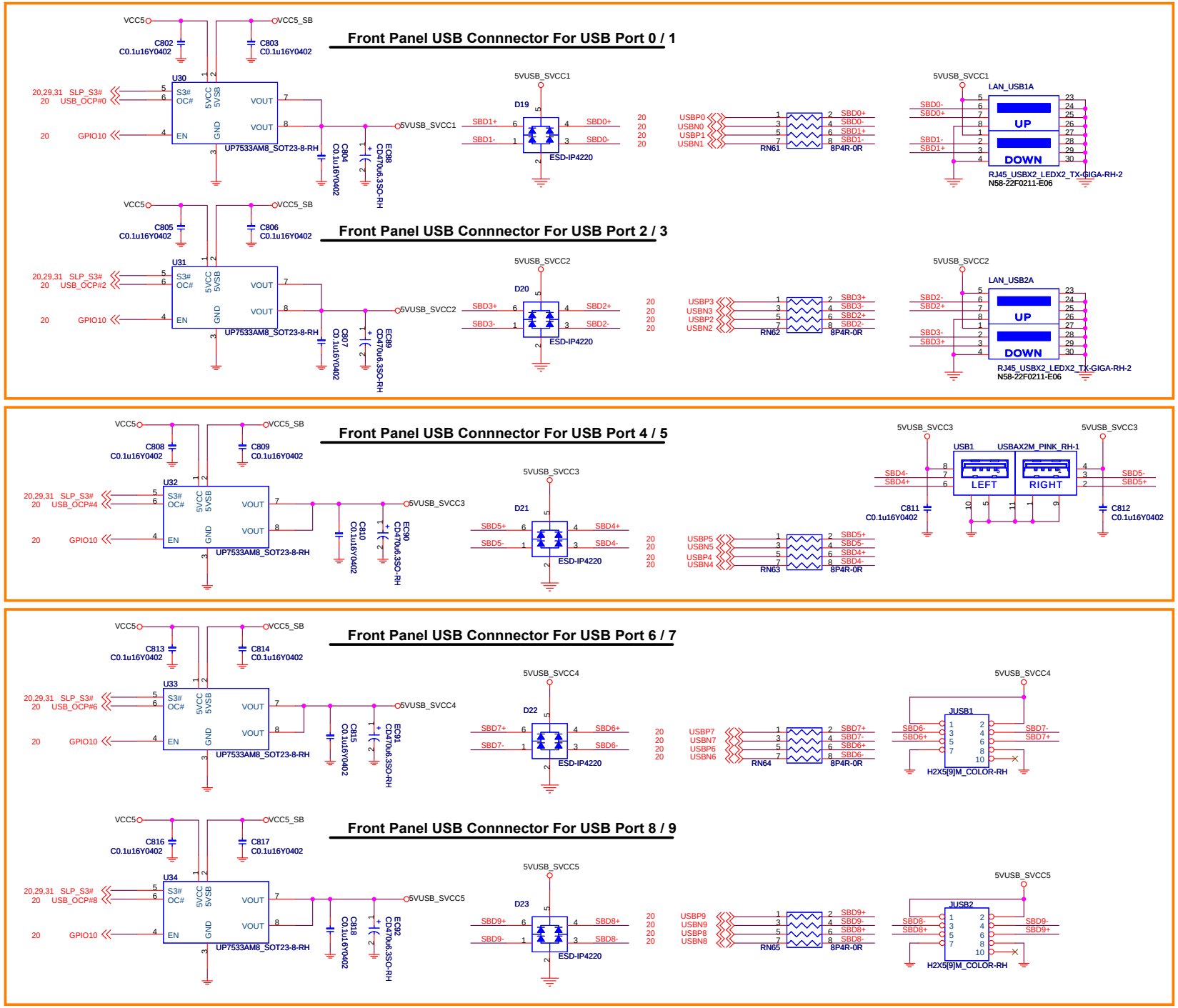
Size	Document Number	Rev
	MS-7510	0A

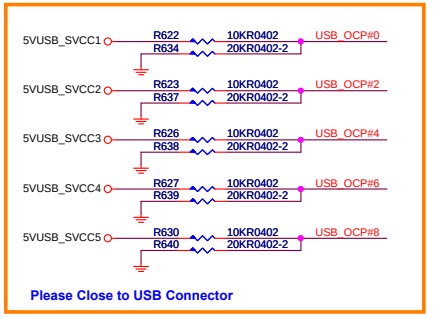
Date: Monday, September 10, 2007 Sheet 32 of 41

Voltage Regular Module (VRD11)



Front Panel and Real I/O USB Connector



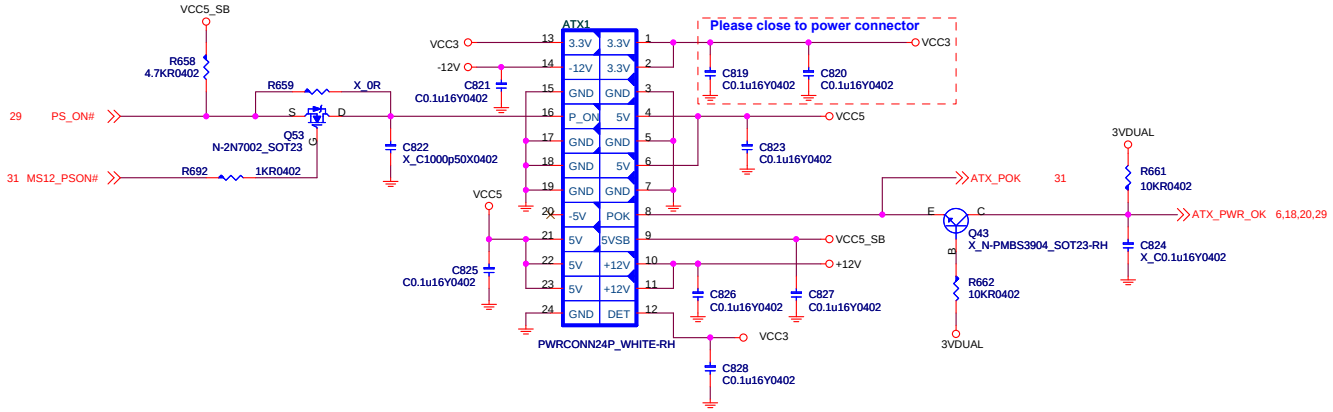


MICRO-START INT'L CO.,LTD.

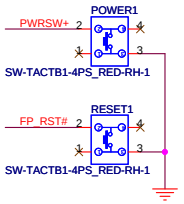
Title	Front / Rear USB Connectors	
Size	Document Number MS-7510	Rev 0A
Date: Friday, September 07, 2007	Sheet 34 of 41	

ATX Power Connector / Front Panel / LED

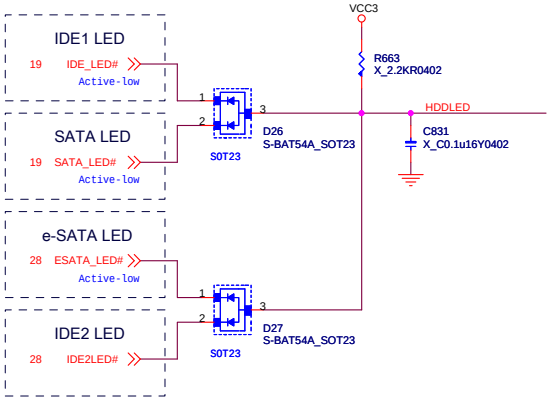
24 Pin ATX Power Connector



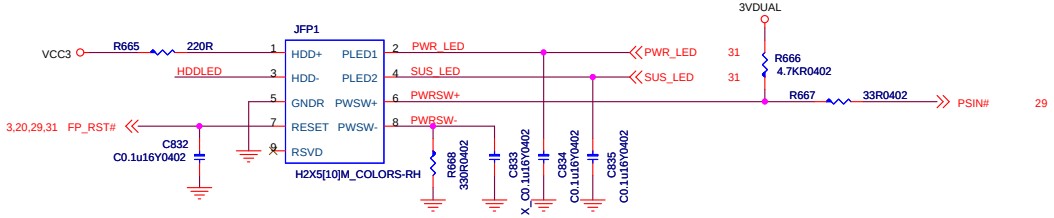
Power and Reset Button

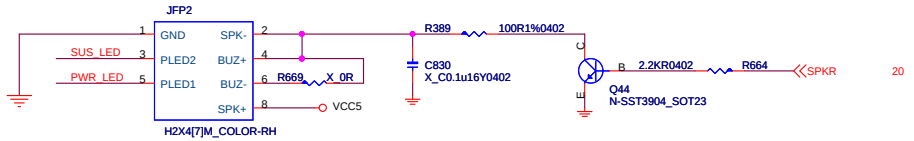


HDD LED

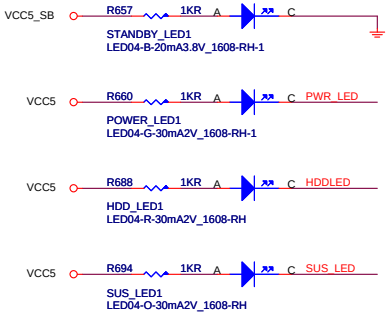


Front Panel



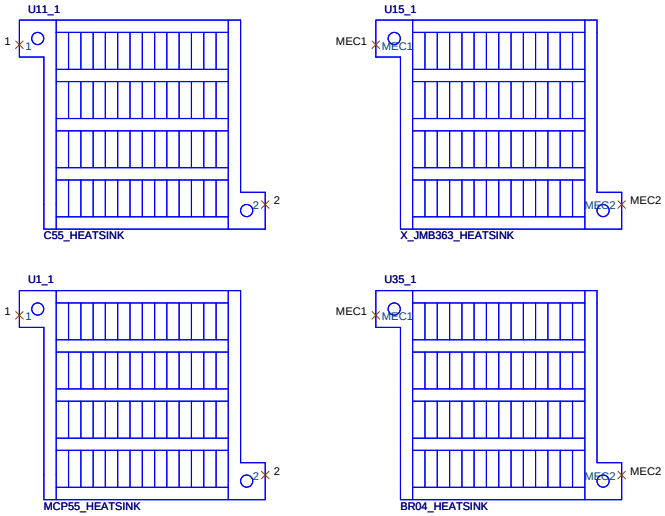


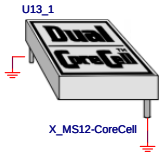
Power State LED

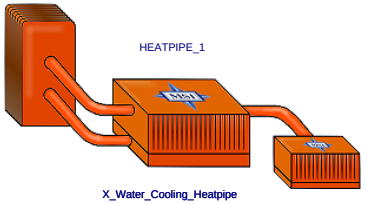


MICRO-START INT'L CO.,LTD.

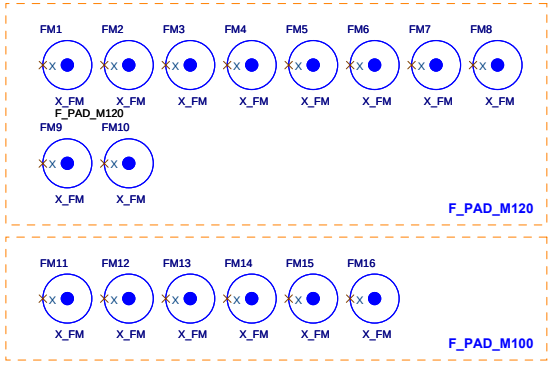
Title: ATX Connector / Front Panel / LED		
Size	Document Number: MS-7510	Rev: 0A
Date: Monday, September 10, 2007	Sheet 35 of 41	



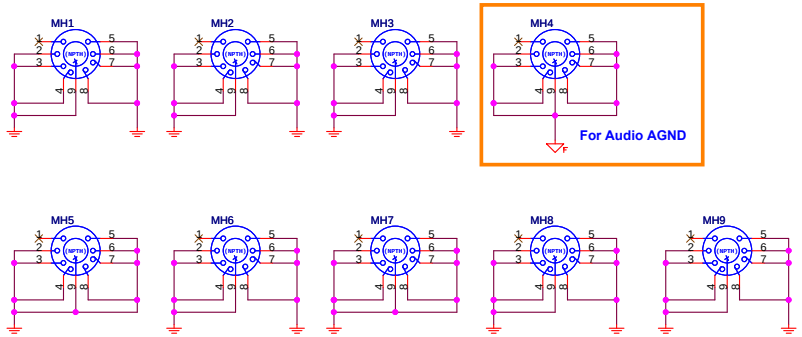




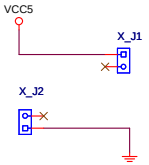
Optics Orientation Holes



PCB Mounting Holes



Simulation



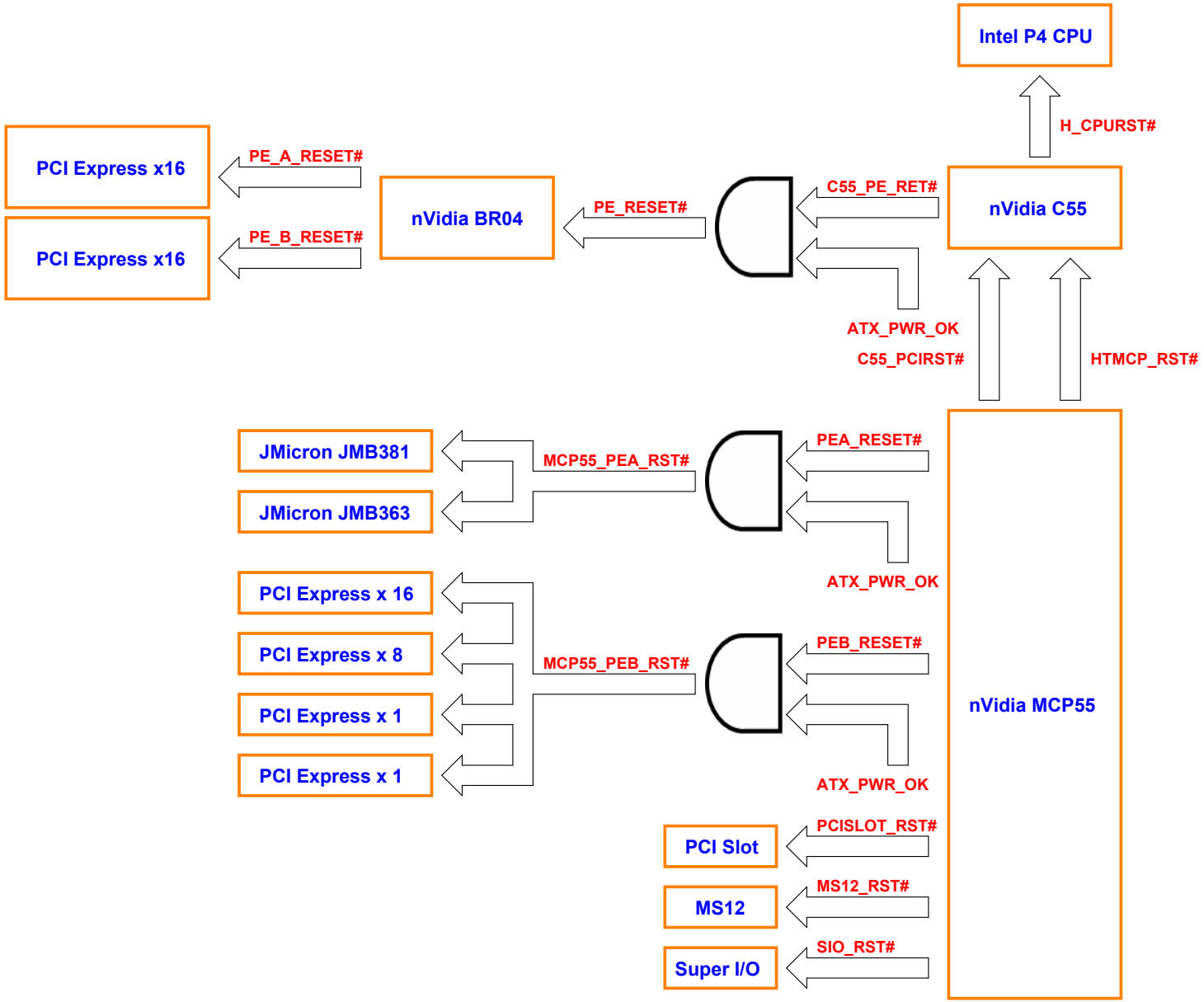
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Manual Parts		
Size	Document Number: MS-7510	Rev: 0A
Date: Monday, September 10, 2007	Sheet 36 of 41	

Power On/Off Sequence

MICRO-START INT'L CO.,LTD.		
Title: Power On/Off Sequence		
Size	Document Number: MS-7510	Rev: 0A
Date: Friday, September 07, 2007	Sheet 37 of 41	

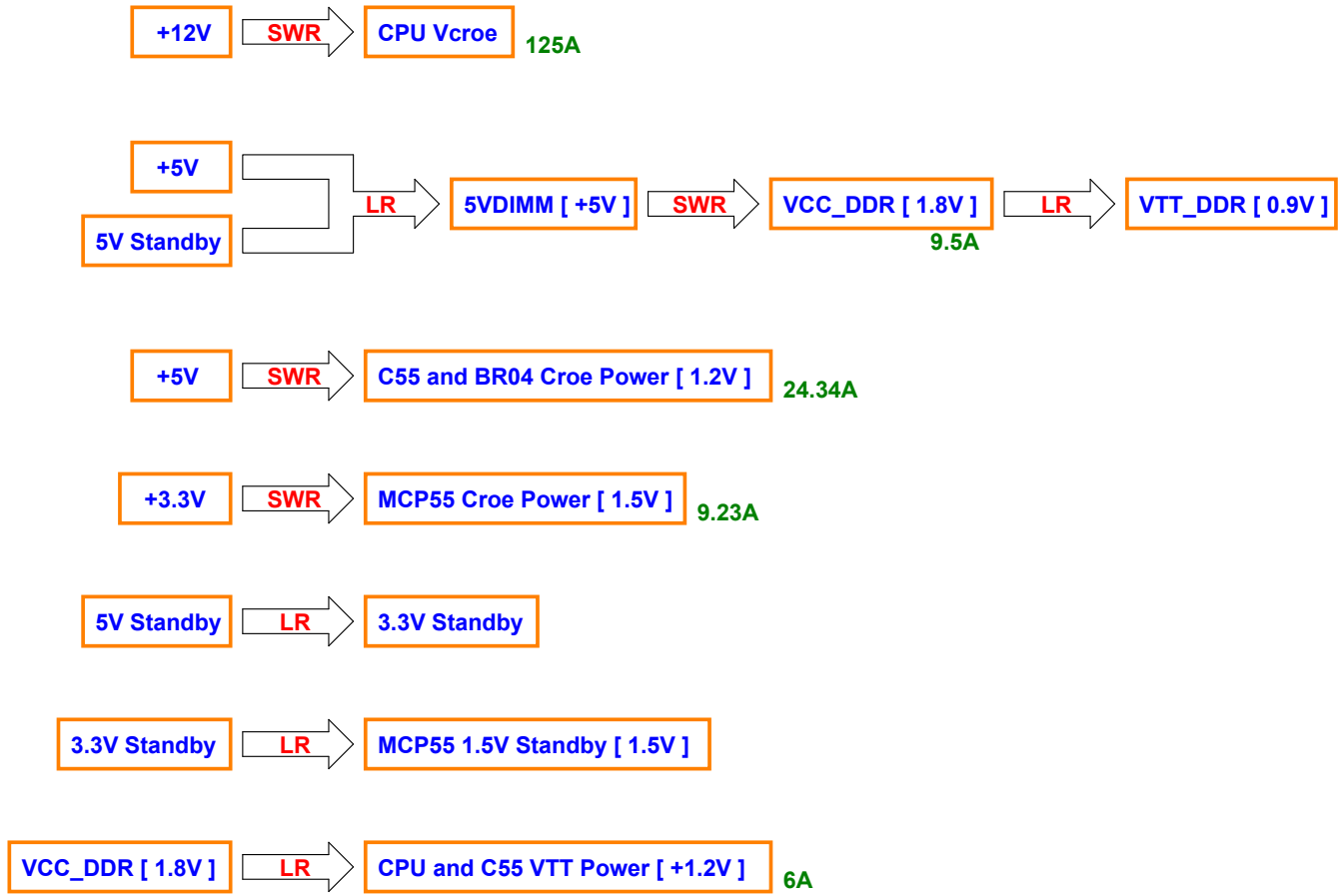
Syatem Reset Map



MICRO-START INT'L CO.,LTD.

Title: Reset Map		
Size	Document Number: MS-7510	Rev: 0A
Date: Friday, September 07, 2007	Sheet 38 of 41	

Syatem Power Map



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Cover Sheet		
Size	Document Number: MS-7510	Rev: 0A
Date: Friday, September 07, 2007	Sheet 39 of 41	

Configuration & GPIO

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	PCI Reset
PCI slot 1	PIRQ#A	PCI0REQ# PCI0GNT#	AD21	PCI_CLK0	PCISLOT_RST#

DDRII DIMM Configuration

DIMM1	DIMM2	DIMM3	DIMM4
A0 1010000B	A4 1010010B	A2 1010001B	A6 1010011B
0A	0B	1A	1B

SMBus Distribution

SMBus	Power	Load
SMBDATA SMBCLK	VCC3	MCP55 , MS12 , PWM , Super I/O , PCI Express x16 Slot * 3 , PCI Express x 8 Slot * 1 , PCI Express x 1 Slot * 1 , PCI Slot
SMB_MEM_DATA SMB_MEM_CLK	VCC3_SB	MCP55

System Reset Signal

Signal	Device
PE_RESET#	BR04
H_CPURST#	CPU
HTMCP_RST#	C55
PE_A_RESET#	BR04 PCI Express x 16 Primary Slot
PE_B_RESET#	BR04 PCI Express x 16 Secondary Slot
PEA_RESET#	Promise PDC42819 SATA/SAS Controller JMicron JMB381 IEEE 1394a Host Controller
PEB_RESET#	MCP55 PCI Express x 16 Slot MCP55 PCI Express x 8 Slot MCP55 PCI Express x 1 Slot
PCISLOT_RST#	MCP55 PCI Slot
C55_PCIRST#	C55
MS12_RST#	MS12 PCI Slot
SIO_RST#	Super I/O

SuperI/O GPIO Function

Pin Name	Function Description
VIDIN0 - VIDIN2	CPU Bus Select Input
VIDOUT0 - VIDOUT2	CPU Bus Select Output
GP7	Reset PWM
GP14	Reset Super I/O
GP15	Use defiult voltage setting
GP16	Use over voltage setting
COPEN#	Detect CPU remove or not

MCP55 GPIO Function

Pin Name	Function Description
GP10	USB Connector OC# Detect

Device Clock Signal

Signal	Device
CK_H_CPU# CK_H_CPU	C55 to CPU
HTMCP_DWNCLK0 HTMCP_DWNCLK0#	C55 to MCP55
HTMCP_UPCLK0 HTMCP_UPCLK0#	MCP55 to C55
PE_BR04_CLK PE_BR04_CLK#	C55 to BR04
PE_A_REFCLK PE_A_REFCLK#	BR04 to Express x 16 Primary Slot
PE_B_REFCLK PE_B_REFCLK#	BR04 to Express x 16 Secondary Slot
MCPOUT_200MHZ MCPOUT_200MHZ#	MCP55 to C55
C55_25MHZ	MCP55 to C55
PE0SB_CLK PE0SB_CLK#	MCP55 to Express x 16 Slot
PE5SB_CLK PE5SB_CLK#	MCP55 to Express x 8 Slot
PE1SB_CLK PE1SB_CLK# PE2SB_CLK PE2SB_CLK#	MCP55 to PCI Express x 1 Slot
PE3SB_CLK PE3SB_CLK#	MCP55 to Promise PDC42819 SATA /SAS Controller
PE4SB_CLK PE4SB_CLK#	MCP55 to JMicron JMB381 IEEE1394a Controller
PCI_CLK0	MCP55 to PCI Slot
SIO_PCLK	MCP55 to FinTek 71883FG Super I/O
LPC_PCLK	MCP55 to JTPM Pin Header

2007-07-25

Crate First Version Schematic

2007-08-08

Net In Schematic

2007-08-22

Update project Spec.
From PDC42819 change to JMB363

2007-09-07

Update nVidia PCI Express clock jitter issue solution

2007-09-12

Gerber Out

MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: ***History***		
Size	Document Number: **MS-7510**	Rev: **0A**
Date: Friday, September 07, 2007	Sheet 41 of 41	